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# TN8000.07

## Technical Note

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### *XE8000 packaging information*

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## 1 INTRODUCTION

This application note describes the packaging of XE8000 circuits.

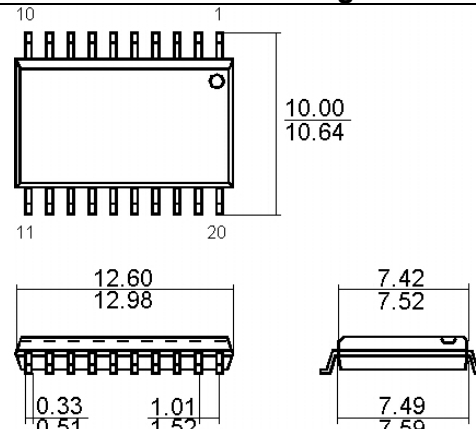
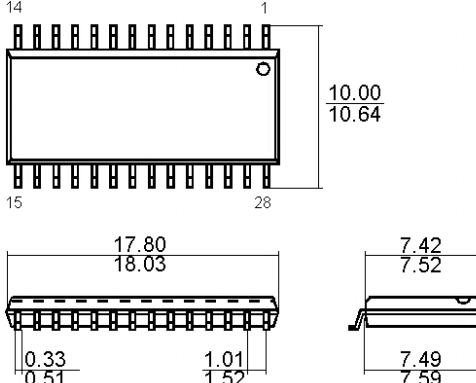
## 2 PACKAGES

The following tables show the package size. All dimensions are in "mm".

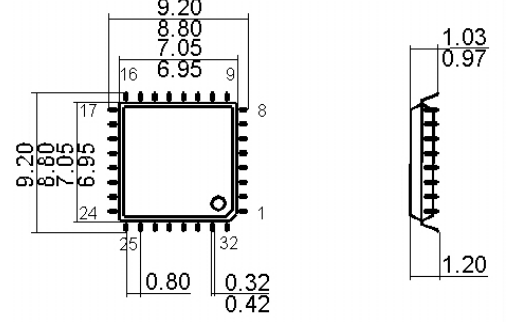
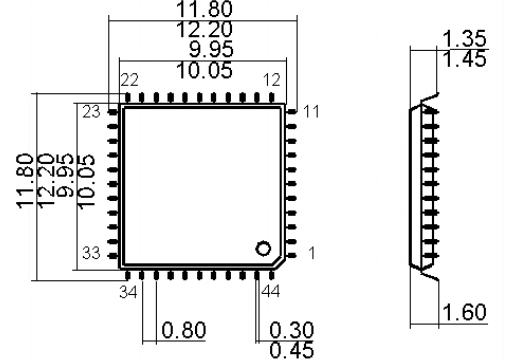
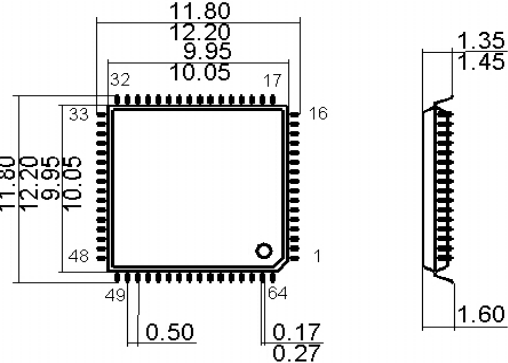
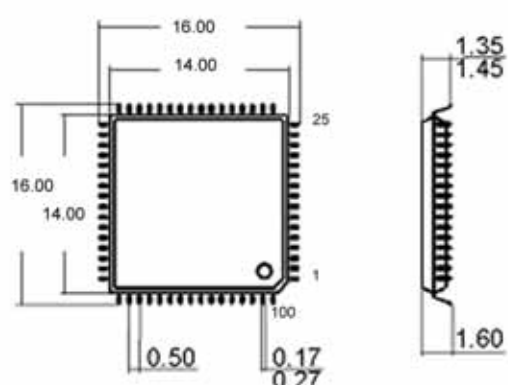
### 2.1 Delivery in die or in wafers

Package extension	Package name	Outline drawings All XE8000 product are currently on 6" wafers
000TW	Bar die in Tested inked Wafers	Complete tested wafers. Not sawn, not back-lapped. Bad chips are marked with a spot of dark ink.
000BF	Bar die on Blue Foil	Complete tested wafers. Sawn, back-lapped, glued on blue tape. Chip must be used within 3 months of wafer delivery. Bad chips are marked with a spot of dark ink.
000WP	Bar die on Waffle Pack	Good chips taken from tested back-lapped wafers and delivered on waffle packs. Number of chips per waffle pack depends on product.

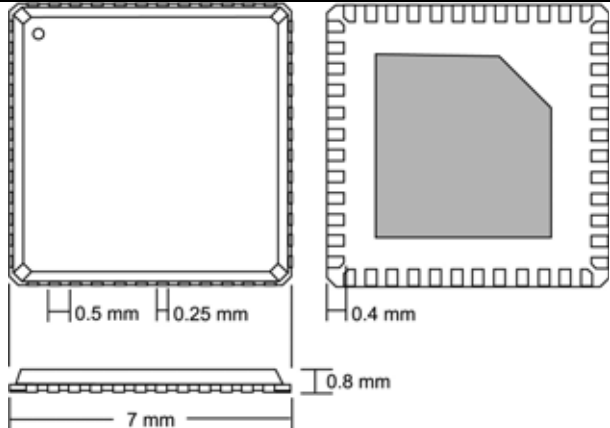
### 2.2 SOIC packages

Package extension	Package name	Outline drawings
012	SO20 SOIC20 SO20WB	 <p>Top view dimensions: 10, 1, 11, 20, 12.60, 12.98, 10.00, 10.64</p> <p>Side view dimensions: 0.33, 0.51, 1.01, 1.52, 7.42, 7.52</p> <p>Perspective view dimensions: 7.49, 7.59</p>
015	SO28 SOIC28 SO28WB	 <p>Top view dimensions: 14, 1, 15, 28, 17.80, 18.03, 10.00, 10.64</p> <p>Side view dimensions: 0.33, 0.51, 1.01, 1.52, 7.42, 7.52</p> <p>Perspective view dimensions: 7.49, 7.59</p>

**2.3 QFP packages**

Package extension	Package name	Outline drawings
026	TQFP32	
027	LQFP44	 <p data-bbox="925 1003 1173 1032">JEDEC MS-026.C</p>
028	LQFP64	 <p data-bbox="925 1406 1173 1435">JEDEC MS-026.C</p>
035	LQFP100	 <p data-bbox="925 1832 1173 1863">JEDEC MS-026.D</p>

**2.4 QFN packages**

Package extension	Package name	Outline drawings
063	VQFN48	 <p style="text-align: center;">JEDEC MO-220.E</p>

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