



# **XE1201A**

# **Transceiver**

## **Databook**

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## Introduction

The XE1201A is a half-duplex FSK single chip transceiver for operation in the 433MHz ISM band and in the 300-500MHz band with a data rate up to 64 kbit/s. The modulation used is the continuous phase, 2 level Frequency Shift Keying (CPFSK).

A serial bus (3 pins) is used to configure the main features of the XE1201A. Transmit, Receive and Enable mode can be set via the 3-wire bus or via two dedicated external pins.

The receiver integrates a LNA, a down converter function as well as channel filtering and demodulator which providing a fully integrated receiver from antenna to data Stream. The architecture used is a direct conversion (zero-If) that provides image filtering. The data stream is processed for a direct micro-controller interface, a synchronized data clock is provided (CLKD pin)

The transmission part provides a complete path from Data stream to antenna. The architecture is a direct up-conversion with a programmable frequency deviation. The RF output power level can also be controlled.

Only few external components are necessary: antenna matching network, tank circuits, saw resonator for local oscillator and low cost crystal.

### Quick Reference Data

Supply voltage	2.4V
RF sensitivity	-109dBm
Data rate	64 Kbit/s
Transmitted power	5dBm
Stand-by supply current	<1uA
Receiver supply current	6mA
Transmission supply current	
	8mA @ 5dBm output power
	5mA @ -10dBm output power

## I - Functional Block Diagram

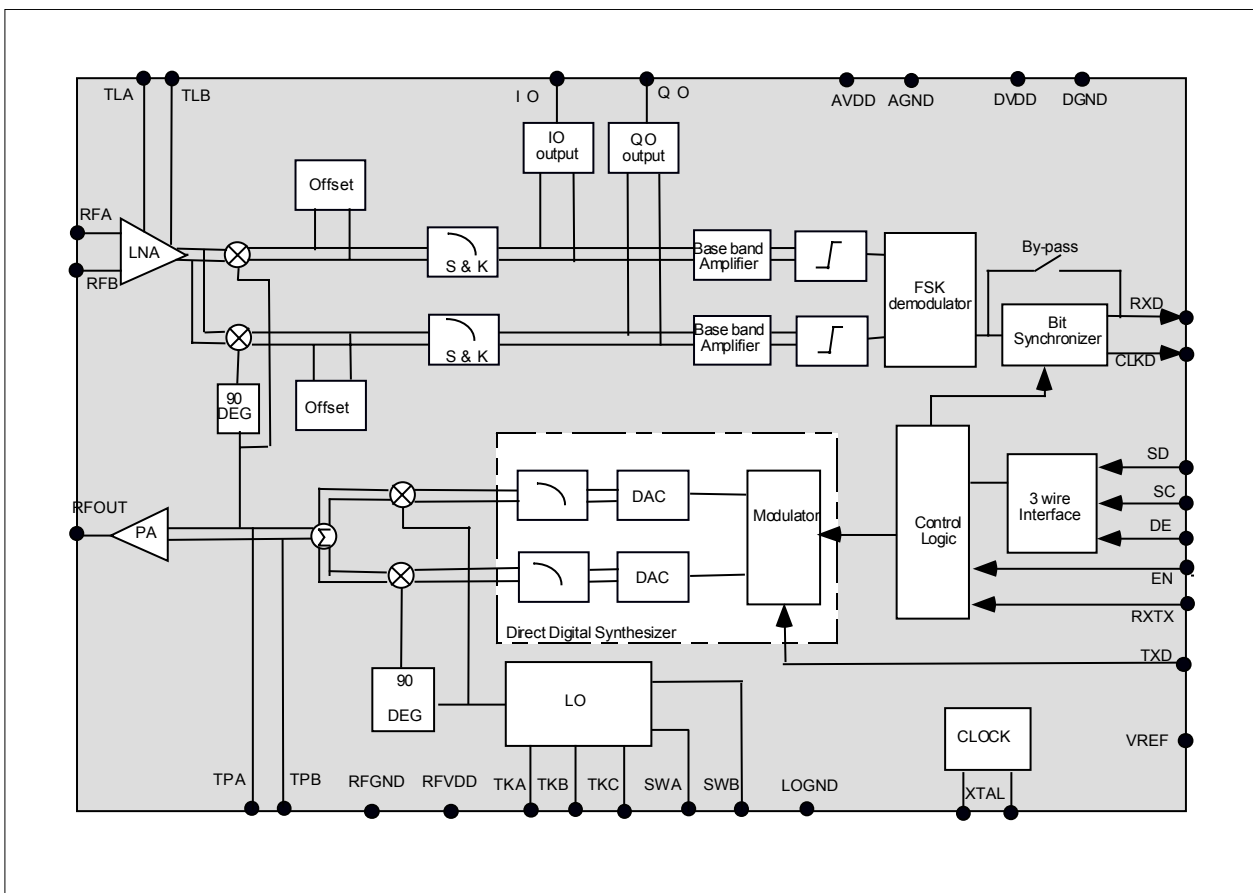


Fig 1 : functional block diagram

## Detailed Pin Description

PIN	NAME	DESCRIPTION
1	EN	Chip enable
2	DE	Bus data enable
3	AVDD	Supply voltage for analog
4	TPA	Power amplifier tank circuit
5	TPB	Power amplifier tank circuit
6	AGND	Ground for analog
7	SC	Bus clock
8	SD	Bus data input
9	LOGND	Ground for local oscillator
10	TKA	Oscillator tank circuit
11	TKB	Oscillator tank circuit
12	TKC	Oscillator tank circuit
13	SWA	SAW resonator
14	SWB	SAW resonator
15	RXTX	Receiver / transmitter enable
16	VREF	Voltage stabilizer decoupling

17	TXD	Data input stream
18	CLKD	Received data clock
19	RXD	Received data output
20	DGND	Ground for digital
21	XTAL	Reference oscillator
22	XTAL	Reference oscillator
23	DVDD	Supply voltage for digital
24	QO	Test pin
25	IO	Test pin
26	RFA	RF input
27	RFB	RF input
28	RFGND	Ground for RF
29	RFOUT	Transmitter output
30	TLA	Low noise amplifier tank circuit
31	TLB	Low noise amplifier tank circuit
32	RFVDD	Supply voltage for RF

## II – Functional Overview

### II-1 High Level description

Receiver:

The modulation used is the Continuous Phase, 2 level Frequency Shift Keying (CPFSK). The RF signal is first amplified with a low noise amplifier before direct conversion: This conversion scheme (zero IF) enables on-chip channel low pass filtering as well as electronic image cancellation avoiding complex and expensive external image filters. The integrated channel filtering is realized with two 4<sup>th</sup> orders Sallen & Key filters. Two self-reception cancellation blocks have been added in I and Q paths in order to prevent from local oscillator self reception problems. The baseband FSK signal is demodulated before digital signal processing in the bit synchronizer block. This block provides glitch free data with synchronized clock so that received data can directly be read by a low cost / low complexity micro-controller.

Transmitter:

The modulator is realized with a Direct Digital Synthesizer (DDS). The I and Q baseband signals are digitally generated before digital to analog conversion. With this method, the FSK frequency deviation is very accurate (accuracy of the crystal oscillator based clock) and can easily be adjusted via the 3-wire bus. After anti-aliasing filtering, the I and Q baseband is directly up-converted to the UHF band. The signal is amplified

with the RF power amplifier. The output power can be adjusted from -20 to -5dBm via the 3-wire bus.

Local oscillator:

The local oscillator is based on a standard SAW (surface acoustic wave) resonator allowing fast switch-on timing. The frequency of this low power UHF oscillator can be changed externally by the SAW resonator.

3-wire bus:

The XE1201A main features can be set by software via 3-wire bus interface. The FSK frequency deviation, clock enable, RF output power and data can be programmed as well as other auxiliary functions. Transmit, receive and stand-by modes can be set either via 3-wire bus or with some dedicated pins.

### II-2 Transmitter

#### II-2-1 Direct Digital Synthesizer Modulator

The modulator is realized with a DDS (Direct Digital Synthesizer). The I and Q baseband signals are digitally generated before digital to analog conversion. With this method, the FSK frequency deviation is very accurate. A frequency offset can also be added to the carrier via 3-wire bus, which allows a local oscillator frequency shift compensation during transmission. The DDS Modulator architecture consists of a digital block and an analog block (*fig2*).

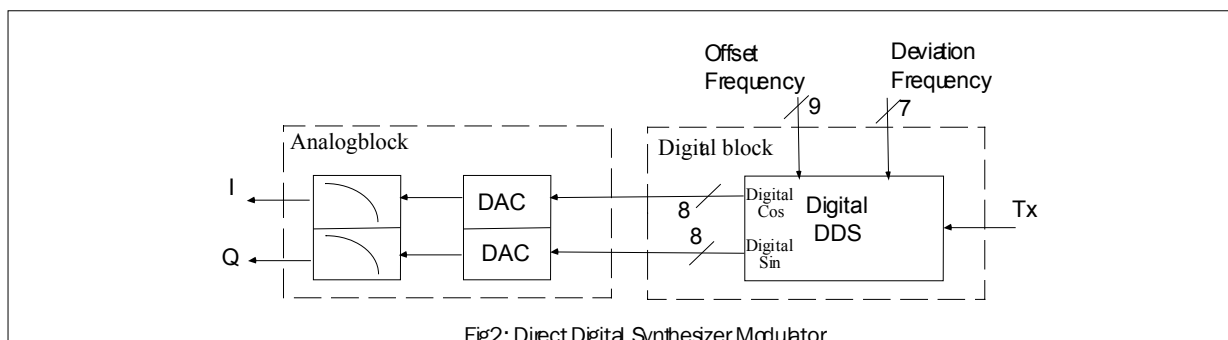


Fig2: Direct Digital Synthesizer Modulator

### II-2-1-1 DDS Digital block

The DDS (*fig3*) converts the data bit stream (TXD pin) into *sin* and *cos* signals. The DDS generates the frequency deviation plus a frequency correction of the local oscillator (offset frequency).

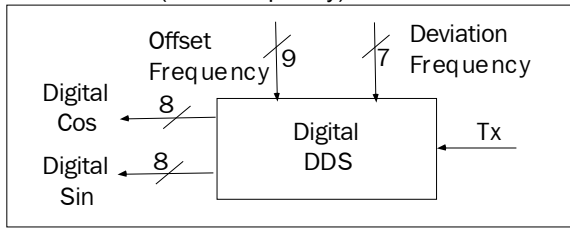


Fig3: DDS Digital block

The system internal clock is set to 2MHz. As the phase accumulator is implemented with 9 bit, the minimum steps, for the frequency deviation and for the offset frequency, is:  $2 \cdot 10^6 / 2^9 = 3.9\text{KHz}$

The frequency deviation (FSK) is programmable. The deviation can be adjusted between 0 and 127 (7bit). Each step corresponds to 3.9KHz. So the theoretical range is 0 to 295kHz. After power-up the deviation value equals 32 (125kHz).

#### Frequency deviation (*fig4*): fdev

If Data = 0 =>  $f_0 - f_{dev}$

If Data = 1 =>  $f_0 + f_{dev}$

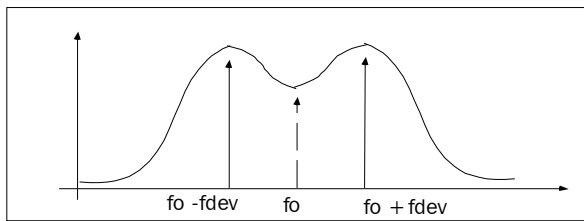


Fig4: Frequency deviation

The 7 bits are used to adjust the frequency deviation of the demodulator according to the following formula:

$$F_{dev} = 3906.25 \cdot n \text{ [Hz]}$$

Where n is the unsigned decimal value of the 7 bits word. It should be noted that for a proper behaviour of the XE1201A demodulator, the frequency deviation must be greater than the data rate and smaller than the receiver filter bandwidth:

$$F_{dev} > \text{Data rate}$$

$$F_{dev} < \text{Filter BW}$$

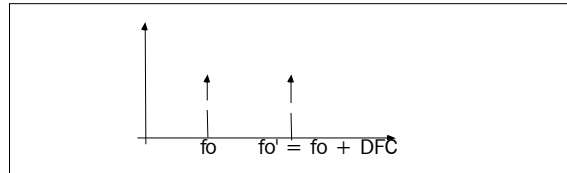
The drift of the Local Oscillator can be compensated, during the transmission via the 3-wire bus, with the offset frequency.

The default setting of the offset frequency is therefore 0. The offset covers +/- 256kHz, with steps of 3.9kHz. The offset value varies between -64 and +63 (in two's complement 7 bit).

#### Positive Offset frequency (*fig5*):

- $f_0$  = frequency of the Local Oscillator (related to SAW resonator initial accuracy)
- DFC = positive offset

Fig5: Positive Offset frequency



#### Negative Offset frequency (*fig6*):

- $f_0$  = frequency of the Local Oscillator (related to SAW resonator initial accuracy)
- DFC = negative offset frequency

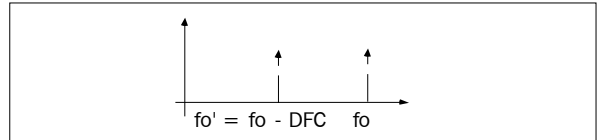


Fig6: Negative Offset frequency

Offset frequency can be calculate according to the following formula:

$$DFC = 3906.25 \cdot n \text{ [Hz]}$$

Where n is the unsigned value

The external Input / Output pins of this block are:

I/O	Name	Function	Pin
Input	TXD	Data input stream	17

Note : The drift of the local oscillateur can not be compensated with the offset frequency (DFC) in receiver mode.

### II-2-1-2 DDS Analog block

The DDSA block (*fig7*) converts the digital sine and cosine words from the DDS into analog I and Q signals. This is accomplished through two 8 bits DA converters followed by Sallen & Key lowpass filters, with nominal cut-off frequency of 160kHz, to remove the aliases components at  $f_s \pm f_0$ , where  $f_s$  is the sampling frequency of 2 MHz and  $f_0$  the output frequency of typically 125kHz.

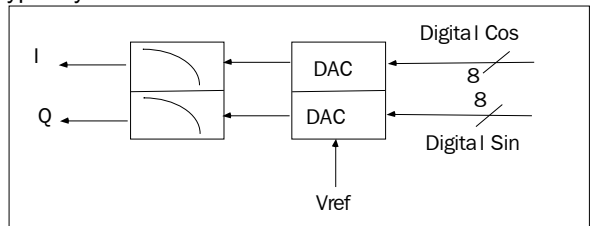


Fig7: DDS Analog Block

The external Input / Output pins of this block are:

I/O	Name	Function	Pin
Input	Vref	Voltage stabilizer decoupling	16

### II-2-2 Single Side Band Up-converter

This block (*fig8*) performs the up conversion of the base-band FSK signal to UHF frequency.

The circuit generates the RF signal driving both the quadrature-down-converter in the receiver path and the power amplifier driver stage in the transmit path.

The single side band modulator is driven by I/Q base-band signal and by LO frequency. The output is a RF

SSB signal. The basic principle of the SSB modulator is to generate one side-band at  $f_{RF} + f_{BB}$  and rejects the image products at  $f_{RF} - f_{BB}$  (or viceversa) An external (discrete) LC circuit tunes this block

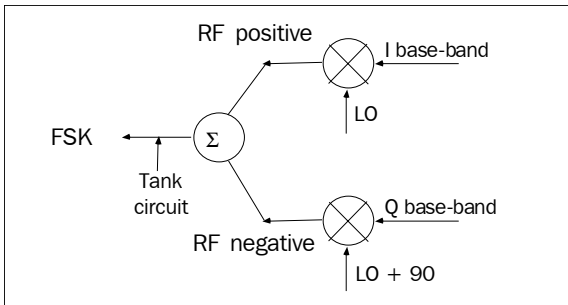


Fig8: Single Side Band Up-converter

External Input / Output:

I/O	Name	Function	Pin
I/O	TPA	PA tank circuit	4
I/O	TPB	PA tank circuit	5

### II-2-3 Power Amplifier

This block provides the RF signal for the transmit antenna. Its inputs are connected to up-converter outputs signal. The PA doesn't drive directly the antenna; an external matching network is required. The output power is programmable: 4 levels are available. Moreover, the output is a current source (open collector): It must be biased to a positive voltage.

External Input / Output:

I/O	Name	Function	Pin
Output	RFout	Transmitter output	29

## II-3 Receiver

### II-3-1 LNA (Low Noise Amplifier)

This block is intended to provide a power gain with a low noise factor. The circuit is inserted between the antenna matching network and the shifter mixer block. It is tuned by two external (discrete) LC circuits: a LC tank circuit connected to the output and a LC matching network connected to the RF input.

External Input / Output:

I/O	Name	Function	Pin
Input	RFA	RF input	26
Input	RFB	RF input	27
I/O	TLA	LNA tank circuit	4
I/O	TLB	LNA tank circuit	5

### II-3-2 Quadrature Down-converters

This block includes a 90 degrees phase shifter and two mixers, one for each channel (I/Q). It performs the direct down-conversion of a 0-IF receiver ( $f_{LO} = f_{RF}$ ). The LO signal comes from the Single Side Band Up-converter output while the RF input is connected to the Low Noise Amplifier output (LNA). The base-band I/Q outputs are connected directly to the base-band analog filtering chain.

### II-3-3 Self reception cancellation block

This block provides a frequency dependant impedance between the IF nodes. It is connected in parallel to each of the mixer output. The circuit attenuates the DC and low frequency output signals of the mixers by 50dB avoiding self reception of the local oscillator.

An active impedance is present between IFP (IF positive) and IFN (IF negative) nodes.

### II-3-4 Baseband Filter

This block performs all the base-band filtering in the receive path. It also provides 20dB of voltage gain. AC coupling (cut-off frequency = 6KHz) avoids offset build-up and attenuates 1/f noise.

The circuit consists of two cascaded filters: 2<sup>nd</sup>-order Sallen & Key low pass stage. Each block provides about 10dB of gain. Together, they implement a 4<sup>th</sup> order Butterworth low pass filter with nominal cut-off frequency of 330kHz. A temperature-compensated resistance reduce the dependence of the transfer function on temperature.

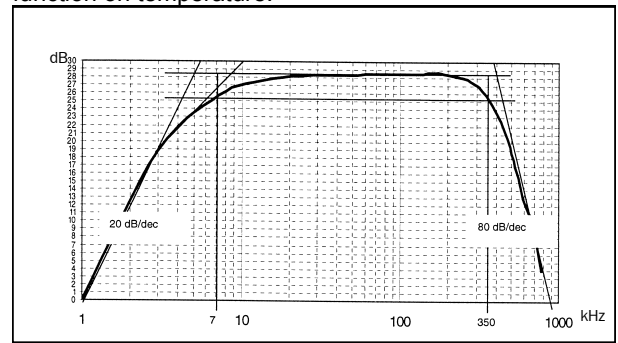


Fig9: Baseband filter

The figure 9 shows that the lower 3dB cut-off frequency is at 7kHz with a 20dB/dec slope and the higher cut-off frequency is at 350kHz with a 80dB/dec slope

### II-3-5 I/Q Analog outputs

This block is intended to convert an analog differential signal into a single ended signal. The analog outputs (I and Q) are used for test purpose or for used of a front-end with another demodulator than the internal one.

Each output is an emitter follower providing output impedance of about 1kΩ.

External Input / Output:

I/O	Name	Function	Pin
Output	IO	Single ended I Test pin	24
Output	QO	Single ended Q Test pin	25

### II-3-6 Baseband Amplifier

This circuit provides 50dB of voltage gain to the base-band filter output signals, thus supplying an adequate signal level to drive the subsequence hard-Limiter.

### II-3-7 Limiter

The circuit Limiter is intended to convert an analog differential signal into a digital signal.

### II-3-8 FSK demodulator

This block (fig10) performs a digital demodulation on the edges of the Limiter outputs. The I and Q signals are demodulated into a bit-stream signal RxD.

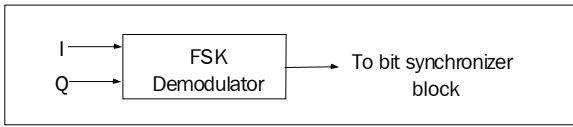


Fig10: FSK Demodulator block

If the bit synchronizer block is not used, the data rate register doesn't need to be set. However, the demodulation performance depends on the index modulation ( $\beta$ ). See table 1.

### II-3-9 Bit synchronizer

This block provides glitch free data with synchronized clock so that received data can directly be read by a low complexity micro-controller.

The operation of a bit synchronizer is based on correlation counters, which integrates the incoming bit stream. The bit-stream RxD and the clock CLKD are synchronized.

The architecture is a digital PLL controlled by an ALU (micro-controller approach) in order to provide a synchronized data clock

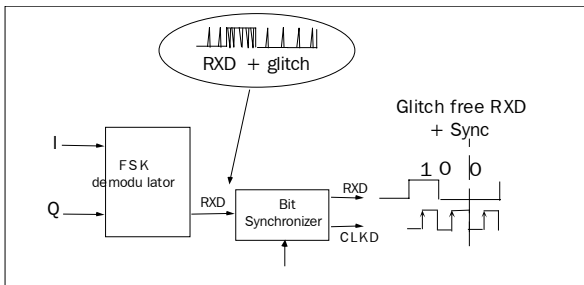


Fig11: Glitch free data + Sync

For a proper behavior, the bit synchronizer must be programmed via the 3-wire bus accordingly to the incoming data rate.

Given a certain desired data rate (in Hz), the user has to enter the digital representation of the integer according to the formula:

$$n = \text{round} \left( \frac{-8 \cdot \log \left( \frac{4.10^6 \cdot DR}{f_{XTAL}} \right)}{\log 2} \right)$$

Where n is an unsigned integer corresponding to 6 bits, and DR is the incoming data rate in (Hz).

Note: The  $4 \cdot 10^6$  is due to the 4MHz external Xtal.

The bit synchronizer can operate with a Data Rate accuracy of  $\pm 5\%$ .

Moreover, the value of the bit rate can influence the receiver sensitivity. The sensitivity depends on the

modulation index  $\beta$  and on the frequency deviation. The following parameters can be defined according to the formulas below:

$$\beta = \frac{f_{dev}}{\text{Datarate}} \quad \text{Or} \quad \text{Datarate} = \frac{f_{dev}}{\beta}$$

The parameter  $\beta$  serves as the modulation index and fdev is the frequency deviation.

These equations show that a relationship exists between modulation index, frequency deviation and data rate. So, the sensitivity depends on the Datarate. The table below and fig 12 show the measure of the sensitivity with a bit error rate less than  $10E-2$  versus modulation index and with a fix Fdev (for example at 125KHz).

Data rate (bit/s)	$\beta$	Sensitivity at BER 1%
1024	122	-112dBm
4873	25.6	-112dBm
9747	12.8	-110dBm
16393	7.6	-108dBm
50564	2.4	-103dBm
60131	2	-102dBm

Table1: XE1201A sensitivity versus  $\beta$  with Fdev =125KHz

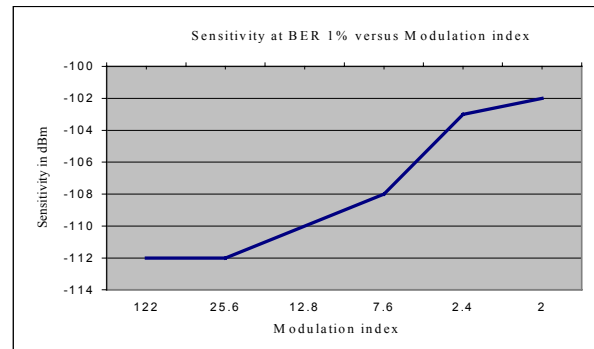


Fig12: Sensitivity at BER 1% versus Modulation index

External Input / Output:

I/O	Name	Function	Pin
Output	RXD	Received data output	19
Output	CLKD	Received data clock	18

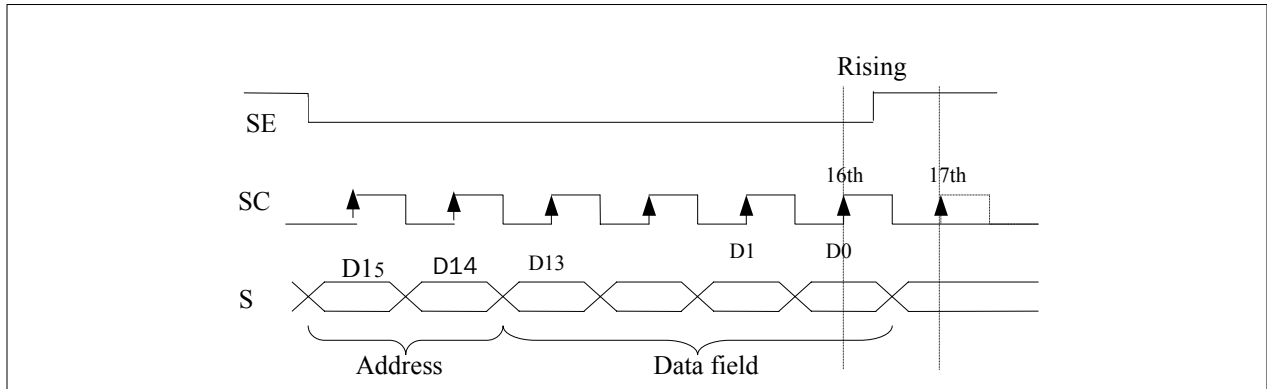


Fig13: Timing diagram

### II-4 Local oscillator

This block generates the local oscillator signal using a high-Q SAW resonator and a low-quality factor LC tank. The SAW resonator determines the oscillating frequency. For an operation in the 433MHz ISM band, typical characteristics for a suitable SAW resonator are:  
 Resonant frequency at 433.92MHz.  
 Unloaded quality: 13000  
 Center frequency tolerance: +/- 75KHz  
 Frequency aging: <+/-10ppm/yr

Reference example :RO2101A (RFM)

The signal generated by this block drives a 90° phase-shifter whose output is connected to a Single Side Band Up-Converter.

External Input / Output:

I/O	Name	Function	Pin
I/O	SAWA	SAW resonator	13
I/O	SAWB	SAW resonator	14
I/O	TKA	LO tank circuit	10
I/O	TKB	LO tank circuit	11
I/O	TKC	LO tank circuit	12

### II-5 Control Logic and 3 wire interface

The transceiver can be set in various configuration modes through the 3-wire interface. This interface consists of a shift register, sampling the data bits on the rising edge of SC (Serial CLK).

This block has an internal circuitry to check the validity of any input. It counts the number of rising edge on serial clock. The data are transferred from the input shift register to the corresponding configuration register, if and only if 16 edges have been detected on the serial clock (SC). After the 16<sup>th</sup> edge, any rising edge on SE (serial enable) will latch the data: A rising edge on SE will latch the data in the configuration register if the internal circuit detects it between the 16<sup>th</sup> and the 17<sup>th</sup> rising edge on the serial clock (fig13).

### II-5-1 Internal Registers

The XE1201A main features can be set by software via 3-wire bus interface and internal registers (Reg A, Reg B and Reg C). The FSK frequency deviation, clock enable, RF output power and data rate can be programmed as well as other auxiliary functions. The first two bits D15 and D14 determine the A, B or C register access according to the truth table below :

D15	D14	Register Name
0	0	Register A
0	1	Register B
1	0	Register C
1	1	Not Used

These three registers are filled by the data A13 to A0, B13 to B0 or C13 to C0 according to the value of D15 and D14. The transmit frame has the following configuration (Table2):

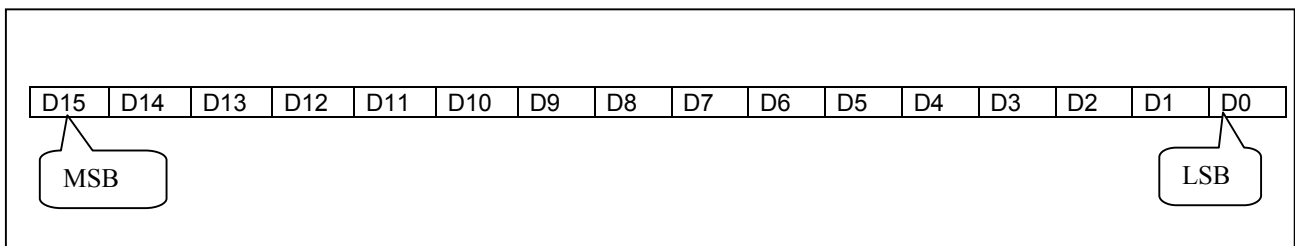


Table2: Internal register

### II-5-2 The register A

This register is used to set the transceiver mode (transmitter mode, receiver mode, stand-by mode) and to select the receiver data rate

To access the register A, D15 and D14 are set to:

- D15 = 0
- D14 = 0

A13	A12	A11	A10	A9	A8	A7	A6
Control Mode	Control CLK	Chip Enable	RXTX	0100=Mode By-pass 0101=Bit sync off			

A5	A4	A3	A2	A1	A0
Receive Data Rate DR=65574*2exp(-n/8)					

### II-5-3 The register B

The register is used for central frequency adjustment during transmission

To access the register B, D15 and D14 are set to:

- D15 = 0
- D14 = 1

B13	B12	B11	B10	B9	B8	B7
Transmitter frequency offset DFC = 3906.25 * n						

B6	B5	B4	B3	B2	B1	B0
Test bits : to be put all at 0						

### II-5-4 The register C

It is used for frequency deviation, enable the power amplifier, transmitted power adjustment and other auxiliary functions.

To access the register B, D15 and D14 are set to:

- D15 = 1
- D14 = 0

C13	C12	C11	C10	C9	C8
PA power		Data inversion bit	Test bit	Test bit	PA Enable
C13	C12				
0	0=-10dBm				
0	1=-5dBm		1	0	
1	0=0dBm				
1	1=+5dBm				

C7	C6	C5	C4	C3	C2	C1	C0
TXD Via 3-wire bus		Transmit frequency deviation Fdev = 3906.25 * n					

### II-5-5 Registers Default values:

After power-up, the internal 3-wire bus registers A, B and C are internally initialized with the following values (Table3):

- Pins control
- CLK stopped
- DR = 16Kbit/s
- PA = -5dBm
- Fdev = +/-125kHz

External Input / Output:

I/O	Name	Function	Pin
Input	SD	Bus data input	6
Input	SC	Bus clock	7
Input	DE	Bus data Enable	2
Input	EN	Chip enable	1
Input	RXTX	Receiver transmitter enable	15

Reg	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>A</b>	0	0	0	0	0	0	0	0	0	1	0	0	0	0
<b>B</b>	0	0	0	0	0	0	0	0	0	0	0	0	0	0
<b>C</b>	0	1	0	1	0	1	0	0	1	0	0	0	0	0

Table3: Registers default values

### III – External Components

#### III-1 SAW Resonator

The SAW resonator determines the carrier frequency. Thus frequency can be chosen between 370 to 470MHz.

A negative resistor is created between SWA and SWB pins with a parallel parasitic capacitor  $C_p$  ( $\approx 3.1\text{pF}$ ). An inductor is placed in parallel (fig14) with the SAW to compensate the influence of the parasitic capacitors  $C_p$  and  $C_s$  ( $C_s$ : Shunt static capacitance of the SAW).

With the SAW resonator RO2101A (RFM) the shunt static capacitance equals  $1.9\text{pF}$ . With thus SAW resonator, the inductor value is:

$L$  nominal =  $27\text{nH}$

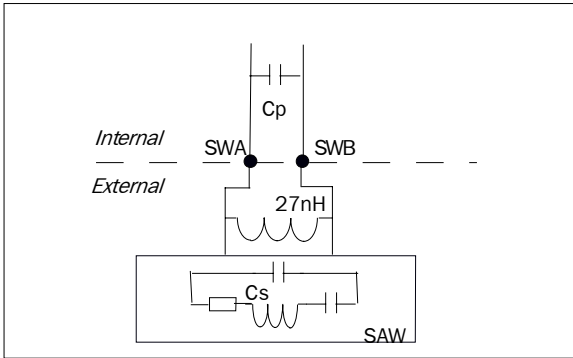


Fig14: Saw Resonator circuit

#### III-2 LNA tank circuit

The function of the LNA tank circuit is to maximize the available power gain (GPAV).

A current source is created between the TLA and TLB pins with a parallel parasitic capacitor  $C_p$ . To compensate the  $C_p$  influence, an inductor  $L$  ( $L_1+L_2$ ) is placed in parallel (fig15).

Moreover, the circuit needs to resonate at  $433.92\text{MHz}$ . This implies the following components values:

$L_1=L_2=12\text{nH}$

$C=2.2\text{pF}$

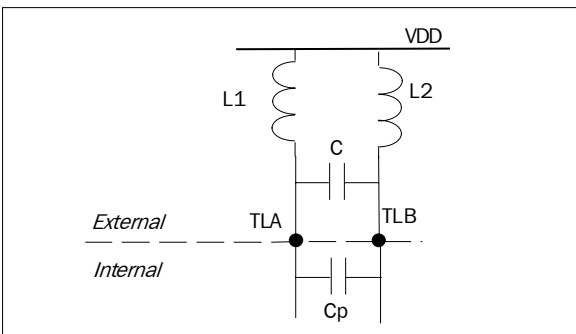


Fig15: LNA tank circuit

Note: The inductors  $L_1$  and  $L_2$  can be printed on the PCB ( $\mu\text{strip}$ )

#### III-3 Up converter tank circuit

The up-converter is used for the transmission path as well as for the receiver path. So if the XE1201A is used as receiver, the up-converter tank (fig16) is necessary.

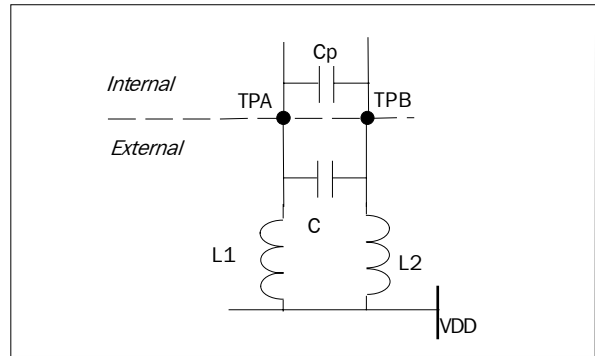


Fig16: Up-converter tank circuit

The Up-converter tank circuit has the same purpose that the LNA tank circuit. However due to different parasitic, the values are:

$L_1=L_2=12\text{nH}$

$C=2.2\text{pF}$

#### III-4 LO tank circuit

The LO must be connected to the following tank circuit (fig17). LC resonance is created between TKA and TKC. TKB (internal biasing) must be grounded via  $C_2$

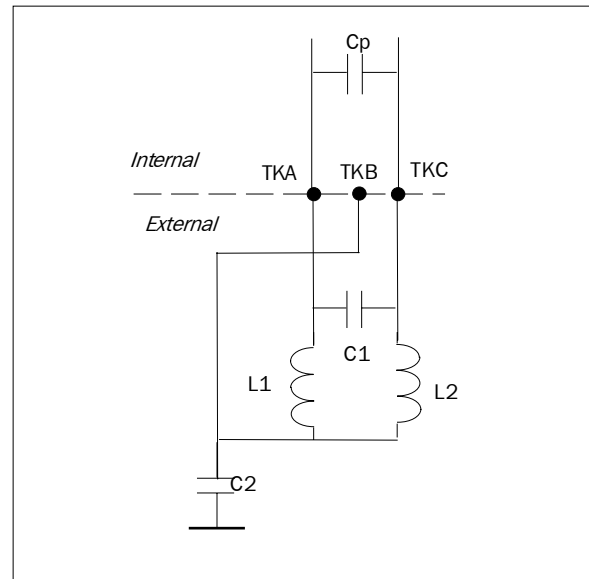


Fig17: LO tank circuit

Resonance :  $(L_1+L_2)(C_1+C_p)\omega^2=1$

External components are defined as:

$L_1=L_2=12\text{nH}$

$C=2.7\text{pF}$

### III-5 Antenna Matching Network

The antenna must be matched and tuned to the transmitter and the receiver to realize good range performance. The Antenna Matching Network consists of:

- RFout Matching Network
- RFin Matching Network
- Switch

#### III-5-1 RFout Matching Network

Topology

A matching network is needed to transmit the maximum power from RFout to the antenna.

The RF output is a current source (open collector like): It must be biased to a positive voltage via an inductor connected to Vdd. The swing is up to twice Vdd.

The maximum of power can be transmitted to a 50Ω antenna if an up-impedance converter (fig18) is realized from 50Ω to 600Ω (RFout impedance = (600+j0) Ω.)

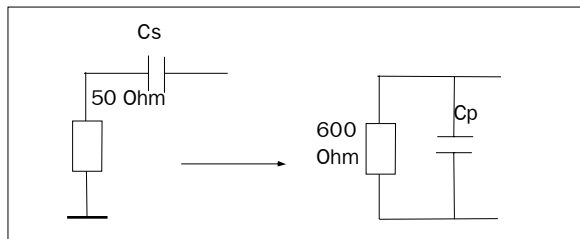


Fig18: Up-impedance converter

The RF out matching network architecture is shown below (fig19):

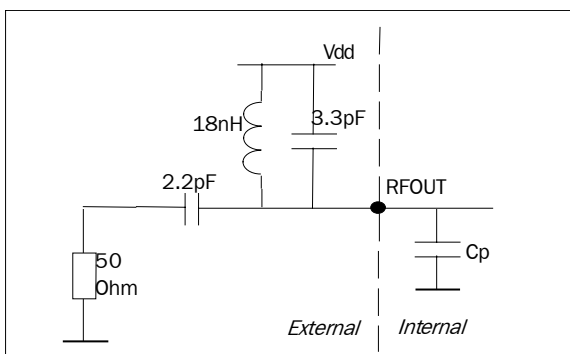


Fig19: RFout matching network

Component Values

The external components can be defined using the Smith chart.

- Start point:  $Z_L = 50\Omega$
- End Point:  $Z_{out} = (600+j0)\Omega$
- Parasitic capacitor  $C_p = 2.4pF$

#### III-5-2 RFin Matching Network

Topology

This function realizes an impedance transform and also single ended to differential transformation. Two input signals are created, one with a phase of  $\pi$ .

The input real impedance of the LNA circuit is  $1k\Omega$ , in parallel model. An up impedance converter is realized from  $1k\Omega$  to  $50\Omega$  at the local frequency

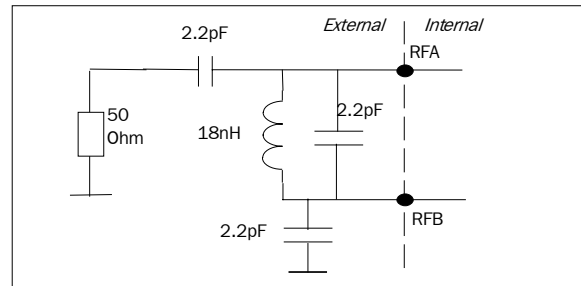


Fig20: RFin Matching Network

Components values

- Input impedance Measure
  - Parallel real part =>  $R_p = 1k\Omega$
  - Parallel capacitor part  $C_p = 4pF$
- Antenna impedance =  $50\Omega$
- $C = 2.2pF$
- $L = 18nH$

#### III-5-3 Switch RFin RFout

Topology

A single antenna can be used for the transmitter and receiver path. It can be realized with a RF switch via two PIN diodes and via a datum (transmitter or receiver configuration)

Switch RFin RFout architecture: (fig21).

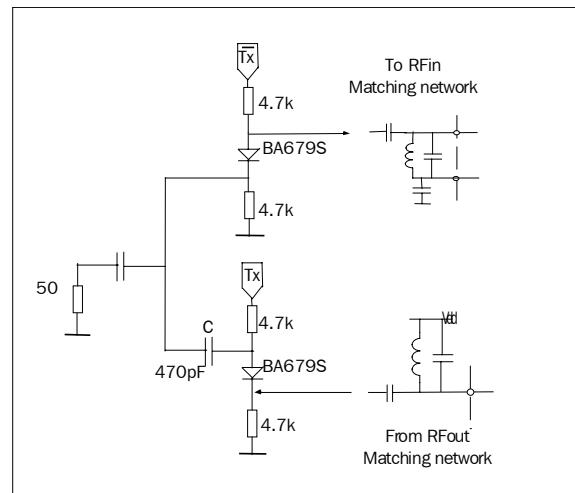


Fig21: Switch RFin RFout

Components values

- Diode PIN Temic : BA679S
- $R = 4.7k\Omega$

The signal (Tx) adds a DC level, a serial capacitor is inserted to eliminate this DC component:  $C = 470pF$

### III-6 Antennas

#### III-6-1 Introduction

The transmission range obviously depends on the antenna performance.

In free space the theoretical equation of the power received  $P_r$  at a distance  $d$  for a wavelength  $\lambda$  is:

$$P_r = \frac{P_t \times G_t \times G_r}{(4\pi d / \lambda)^2}$$

Where  $P_t$  is the transmit power. This power is increased by a factor called *antenna gain* ( $G_t$ ).

The received power ( $P_r$ ) depends of the receiving gain antenna ( $G_r$ ).

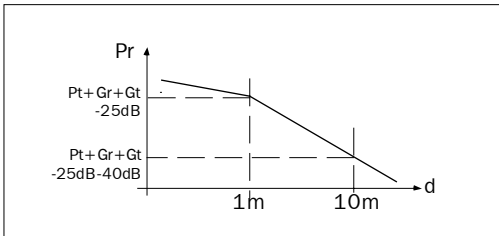
The commonly admitted model is:

- For distance less than 1 meter, the model is  $1/d^2$ .

$$Pr(dB) = Pt(dB) + Gt(dB) + Gr(dB) - 20 \log(4\pi d / \lambda)$$

- For distance longer than 1 meter, the model is  $1/d^4$ .

$$Pr(dB) = Pt(dB) + Gt(dB) + Gr(dB) - 25dB - 40 \log(d/1m)$$



#### III-6-2 Range calculation example

The receiving power required for a  $10^{-2}$  Bit error rate is -109dBm. The power transmit is +5dBm without external power amplifier and +10dBm with external PA. Assuming  $\lambda/4$  antenna gain of -10dBi (easily achievable) the range is:

- In free space (with  $1/d^2$  attenuation model)
  - Without external PA  $d=870m$ .
  - With external PA  $d=4900m$ .
- In building (with  $1/d^4$  attenuation model)
  - Without external PA  $d=30m$
  - With external PA  $d=70m$

#### III-6-3 Whip antenna

The whip antenna (*fig22*) is the simplest. This is a quarter wavelength wire that stands above a groundplane

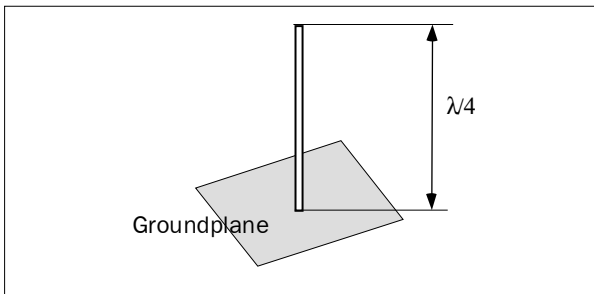


Fig22: Whip antenna

The size whip is defined by:  $l = \frac{\lambda}{4} = \frac{c}{4f_0}$

Where  $f_0$  is the carrier frequency,  $\lambda$  the wavelength and  $c$  the celerity of light.

For an in-ISM-band application  $f_0=433.92MHz$  and

$$l = \frac{3 \times 10^8}{4 \times 433.92 \times 10^6} = 17.2cm$$

These antennas have a gain between -10dBi up to 0dBi.

#### III-6-4 Small rectangular antenna

The loop element can be composed of thin wire, a thin plate element, printed wire or other materials. All are very simple, compact, light weight, low cost and unbreakable.

One advantage is that hand effects do not easily detune the loop. The loop can be made small, is not groundplane dependent. For these reasons, loop antennas are very common in portable applications.

The disadvantage is that small loop antennas have a poor gain (-20dB up to -5dB) and a very narrow bandwidth, this makes critical tuning. The tuning is often done with a variable capacitor, which adds to the cost. If the loop is large, a non-variable capacitor can be used.

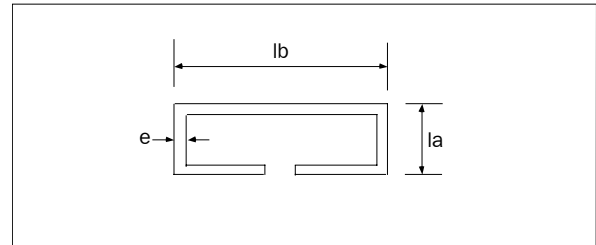


Fig23: loop antenna

The system gain  $G$  ( $G_r$  or  $G_t$ ) of a loop antenna shown below is function of the frequency, the loop area  $A$  is taken as the parameter.

Where  $A$  is defined as:  $A=la*lb$

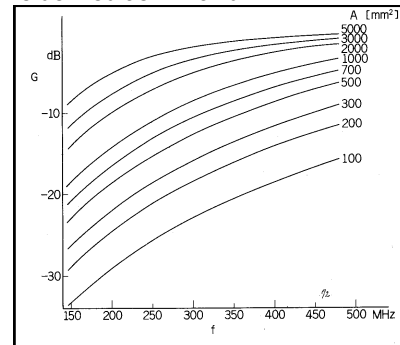


Fig24: Gain versus surface

#### III-7 Adjustment

XE1201A based applications must be trimmed to the carrier frequency with the Local Oscillator tank circuit trimmer capacitor: The Local Oscillator frequency can be picked-up at the RFout port, with a spectrum analyzer.

Capacitor of the LNA and PA tank circuit do need to be trimmed if a low-quality factor is used

If necessary,  $Q$  can be degraded with a parallel resistor.

## IV – XE1201A Performances

### IV-1 Test set-up

These test set-up series are done with a controlled Bit Error Rate (BER) better than 10E-2 and 16 bit of pattern in the receiver chain.

An FSK signal is connected to RFin. RxD (pin19) is the received data output and CLKD (pin18) the received data clock.

The circuit is programmed in receiver mode:

A13=1            A11=1            A10=1

The test set-up is shown *figure 25*

- Sensitivity (*fig26*) versus FSK deviation @ 64kbit/s with a BER<1%

With a FSK deviation less than 75kHz, the sensitivity is better than -102dBm. The typical value is 125kHz. The maximum is 300kHz due to the receiver filter. If the FSK signal is generated by the XE1201A, the maximum frequency deviation is 160kHz before attenuation by transmitter anti alias filter.

- Sensitivity (*fig27*) versus carrier frequency Data rate :16Kbit/s

The sensitivity is maximum (-109dBm) for a carrier frequency around 433.92MHz. A sensitivity under -100 dBm allows a frequency band of 100MHz (370 – 470MHz).

### IV-2 Adjacent channel rejection

Method of measurement: *figure 28*.

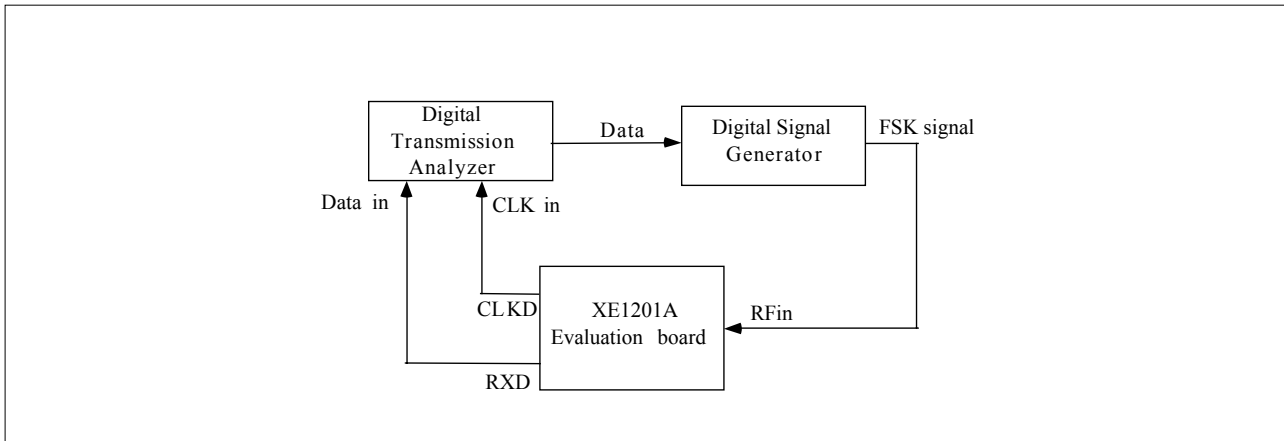
The FSK signal input power value is -105dBm.

Curve *fig29* shows that 40dB rejection is achieved for unwanted signal at 1MHz from the carrier frequency.

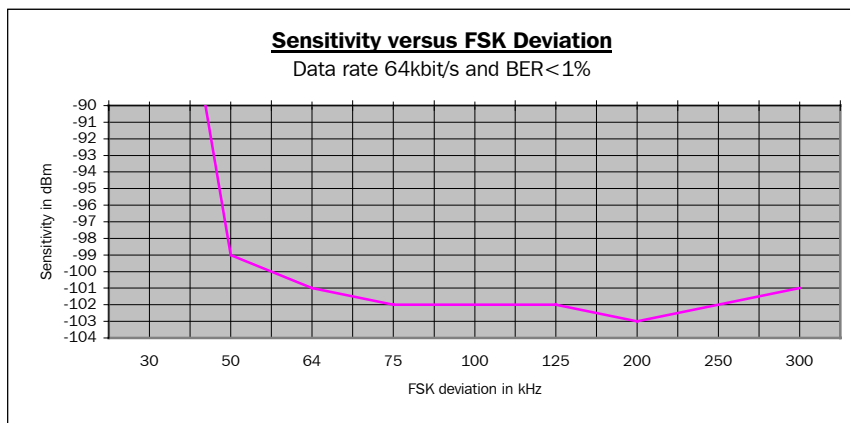
### IV-3 Offset frequency

A frequency offset can be added to the carrier frequency in transmission mode to compensate the drift of the local oscillator.

A frequency of +/-100kHz can be added without degrading the sensitivity *fig30*.



*Fig25: Test set-up, method of measure*



*Fig26: Sensitivity versus Carrier frequency*

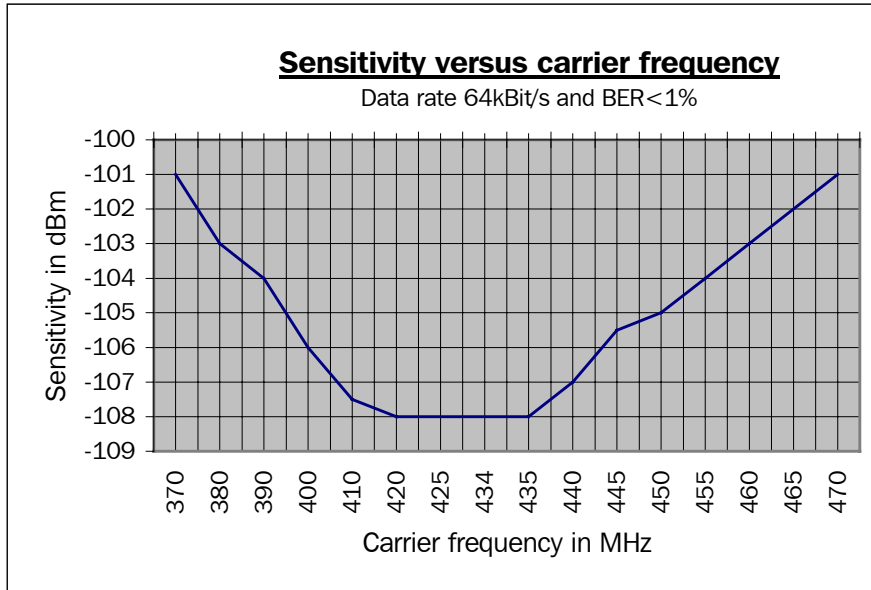


Fig27: Sensitivity versus Carrier frequency

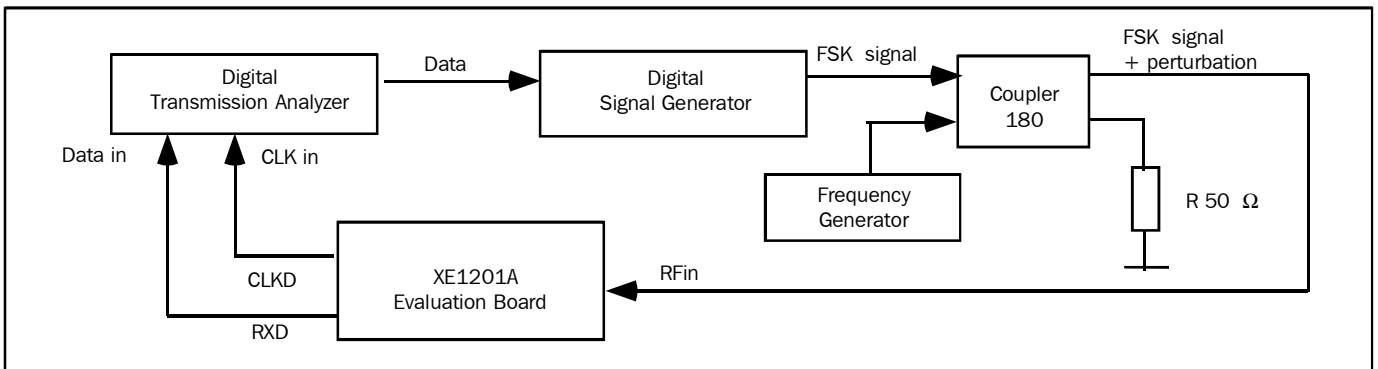


Fig28: Adjacent channel rejection, Method of measure

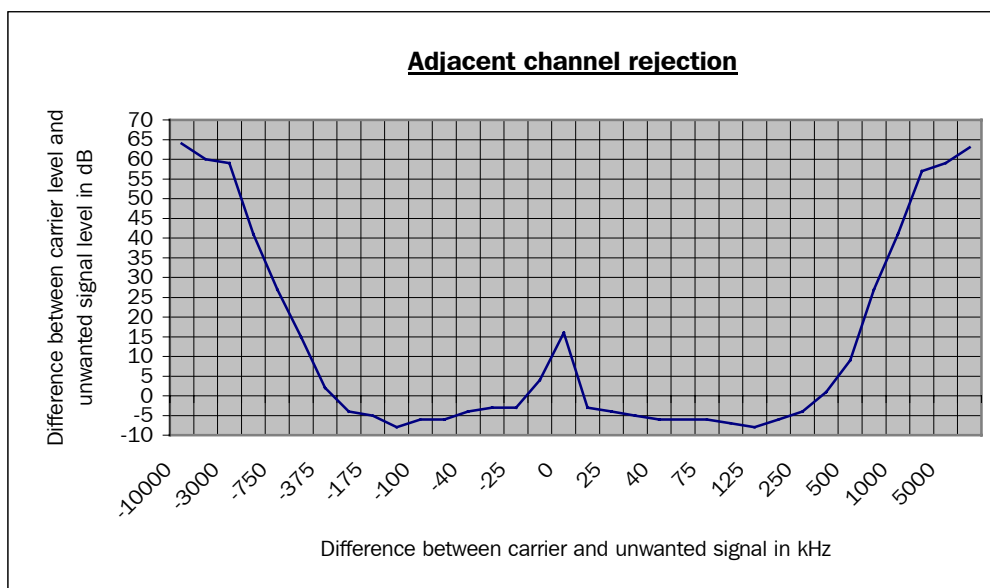


Fig29: Adjacent channel rejection

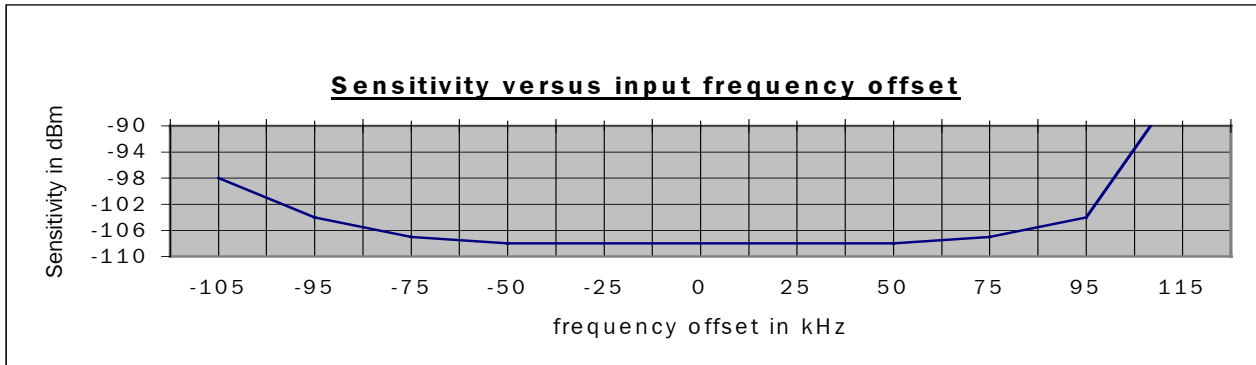


Fig30: Sensitivity versus input frequency

#### IV-2 Waveforms

Rx data output in receiver mode:

The waveforms below show the benefit of the bit synchronizer function. On figure 31, for a RF input level at -102dBm and bit synchronizer by-passed, a relatively complex micro-controller is required for clock

recovery. On figure 32, with the same RF input level and bit synchronizer used, glitch free data are synchronized with the data clock and can be directly read by a low complexity/ low cost micro-controller without any external signal processing

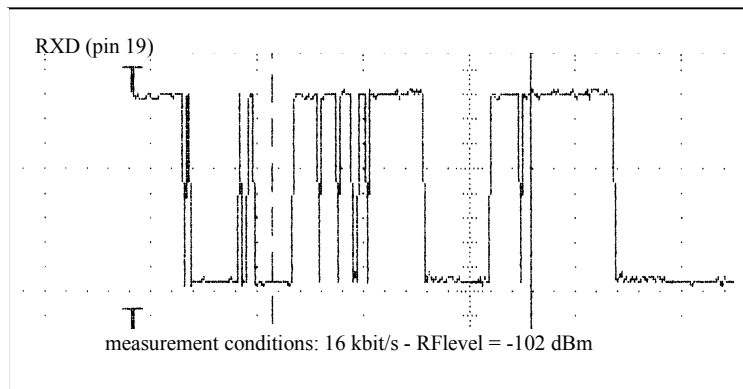


Fig31: Received data stream with internal bit synchronizer bypassed

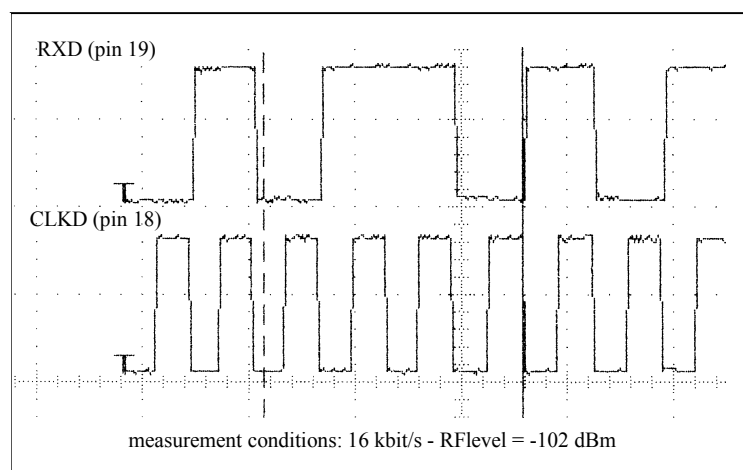


Fig32: Received data stream with internal bit synchronizer and synchronized data clock output

### IV-3 Smith Chart

#### IV-3-1 Input impedance

The figure33 shows the input impedance RFin of the transceiver. The different values of S11 are used to realize a good matching network at the carrier frequency.

- Marker 1 =300MHz →(21-248j) Ω
- Marker 2 =2GHz →(15-60j) Ω
- Marker 3 =433.92MHz →(19-170j) Ω
- Marker 4 = 800MHz →(16-86j) Ω

#### IV-3-2 Input application board impedance

This measurement fig34, corresponding to the input board impedance. It shall be noted that the matching network is adjusted for 433.92MHz.

The real part and the imaginary part of S11 are in the table below

Frequency in MHz	Series impedance in Ω
300	2-120j
400	10-45j
433.92	50+20j
500	24-124j

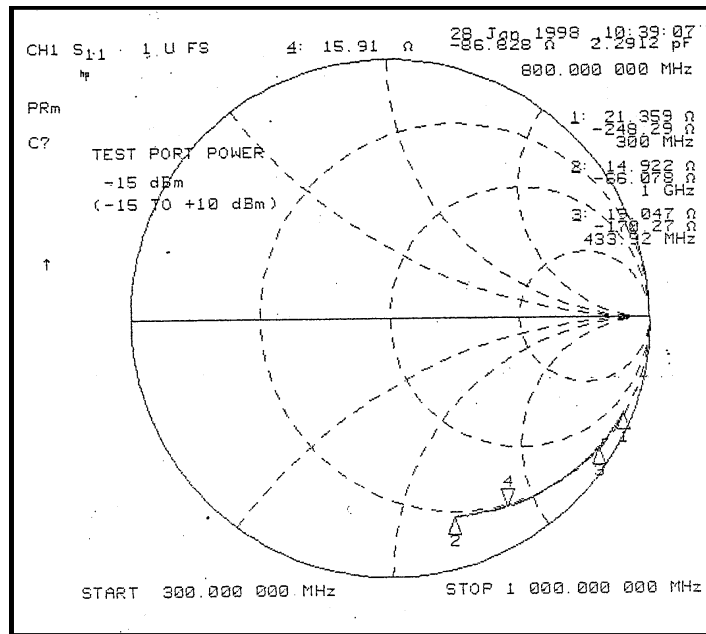


Fig33: Input impedance Rfin ( S11)

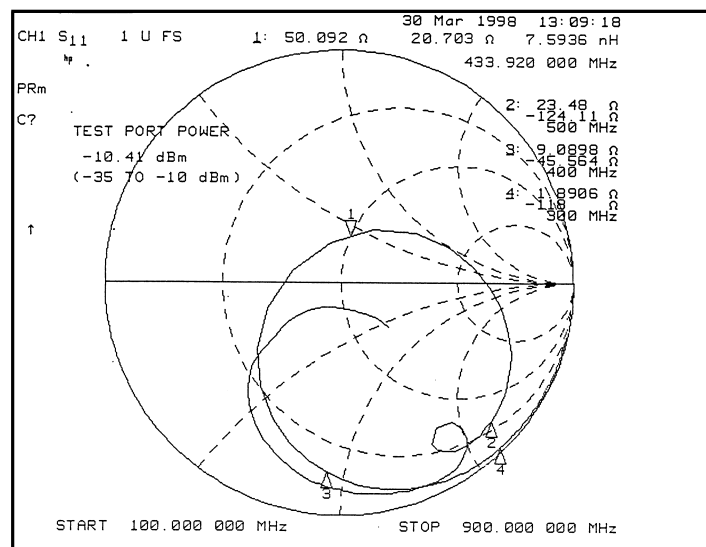
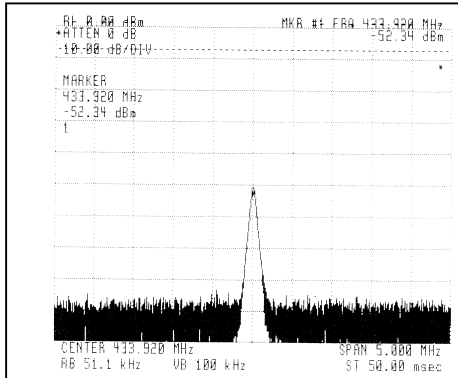


Fig34 :Input impedance RFin of evaluation board

## IV-4-Spectrum waveforms

### IV-4-1 Local oscillator spectrum

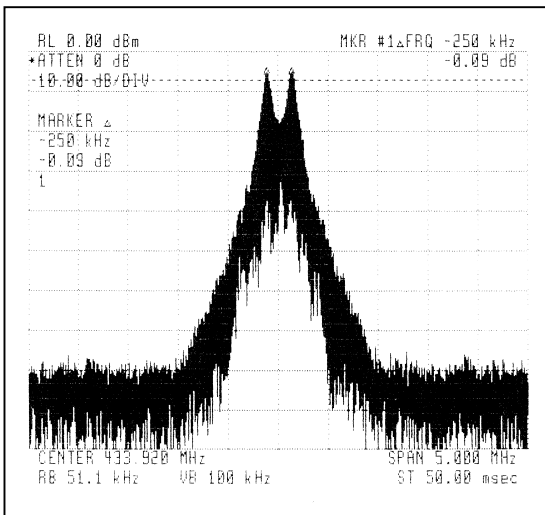
When the transceiver is configured as receiver, the LO can be observed (*fig35*) at 433.92MHz on RFout (level=-50 dBm). This signal is also present on RFin, (level=-73 dBm) this is caused by leakage of the Local oscillator.



*Fig35: Local oscillator Spectrum*

### IV-4-2 RFout spectrum

The *figure 36* shows the spectrum of a FSK signal measured at transmitter output. A pseudo-random bit sequence is applied on the Tx pin of the transceiver. The frequency deviation is set to 125kHz ( $\Delta$ marker = 2fdev =250kHz). The transmit power is set to -5dBm. Out of the ISM band spurious signals are below 60dB.

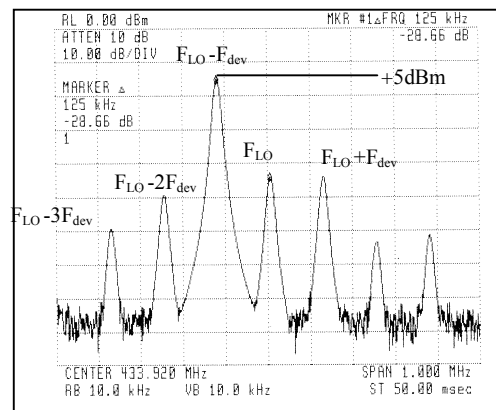


*Fig36: FSK spectrum*

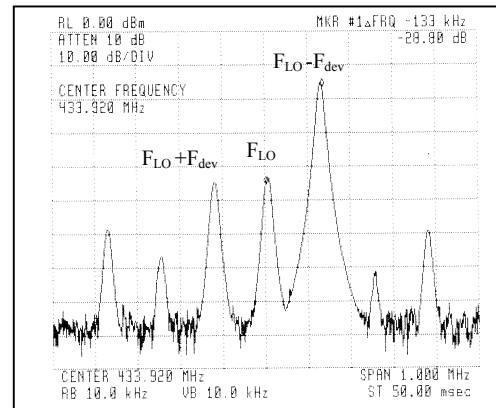
### IV-4-3 Static FSK spectrum

The *figure 37* shows the spectrum of a FSK signal for 0 transmit ( $F_{LO}-F_{dev}$ ) and the *figure 38* for a 1 transmit ( $F_{LO}+F_{dev}$ ). In static mode the attenuation of the spurious of the 3<sup>rd</sup> harmonic of fdev are better than 40dB.

- LO feed through is measured at -29dBc
- Fdev image at 30dBc
- 2<sup>nd</sup> harmonic < 50dBc
- 3<sup>rd</sup> harmonic < 40dBc



*fig37: "0" transmit*



*fig38: "1" transmit*

## V – Application Example

### V-1 Principe

The *figure 39* gives an overview of an application example

A base station sends information to portable receivers. Each receiver is identified by an ID code (for example IDcode=1, 2 and 3)

The link characteristics of this application are:

- Battery saving cycle for all the receivers
- Data rate 64kbit/s
- Response time maximum: 1s
- Transmitted output power: +5dBm
- Frequency deviation: 125kHz

### V-2 Protocol definition for the receiver

To optimize the battery life, all the receivers are in stand by-mode and switch to receiver mode every 1s (*fig40*). If no transmission need to be realized, the receiver returns to stand-by mode. The receivers need to see a preamble, a pattern frame and the ID code (*fig41*).

- Preamble uses to synchronize the data clock
- Pattern uses to identify the *begin of transmission* and authorize it.
- ID code uses to identify the receiver.

The pattern processing is made by a micro-controller.

The rules are described in the following table.

Pattern identified	Mode
Yes	Receiver mode maintained
NO	Switch to stand-by

In receiver mode, if no pattern is received or identified, the receiver switches to stand by mode. If the micro-controller identifies the pattern, the receiver mode is maintained and the data are processed (*fig42*).

The micro-controller needs the synchronized clock, which is generated by the bit synchronizer, for the pattern processing. In this case, the receiver must demodulate the preamble frame for the synchronized data clock generation (*fig43*).

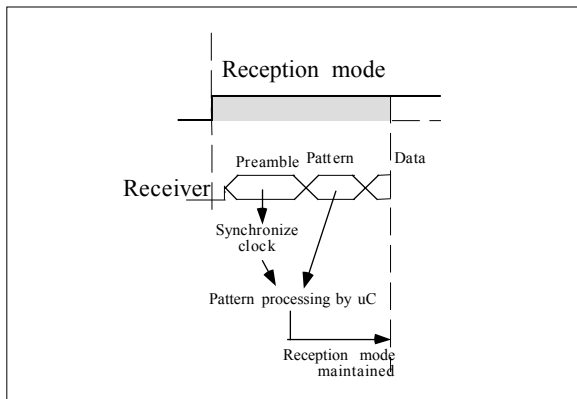


Fig43: Timing for Pattern processing

In this system, two conditions are necessary:

- The receiver needs to demodulate an entire preamble frame to generate the synchronized clock.
- The receiver needs a complete pattern frame for identification.

If one of them is not respected, the receiver mode is not maintained and the receiver switches to stand-by mode.

The figure (*fig44*) below shows two worst cases of pattern processing:

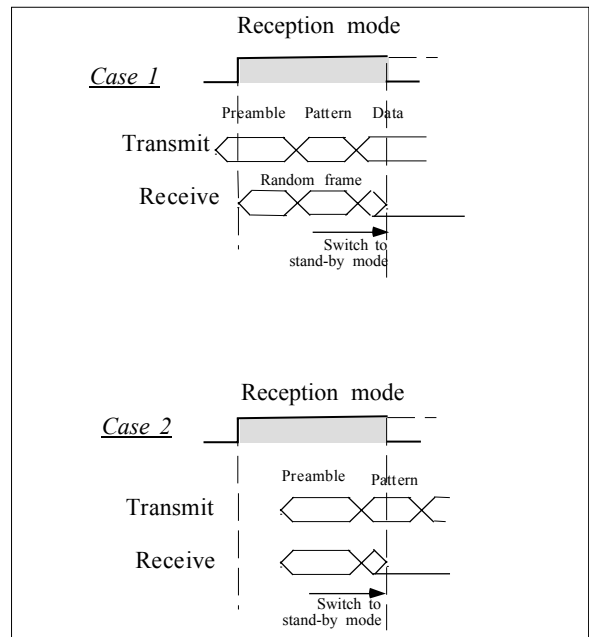


Fig44: Pattern processing worst case

- Case 1: All the bits of the preamble are not demodulated completely so the bit synchronizer can not generate the synchronized clock. The result is that the micro-controller can not identify the pattern. The receiver switch to stand-by mode
- Case 2: The bit synchronizer generates a synchronized clock with the preamble frame but the micro-controller can not identify the entire pattern frame. The receiver switches to stand-by mode

The following configuration (*fig45*) eliminates the problem. The protocol frame must be a sequence of pattern and preamble sent alternatively. The receiver mode time must be longer than two preamble and two pattern frames. In this condition, the receiver does not switch to stand-by mode if a transmission needs to be realized.

This implies the following equations:

$$T_{rm} \geq 2 \times (T_{preamble} + T_{pattern})$$

Where  $T_{rm}$  is the minimum receiver time.

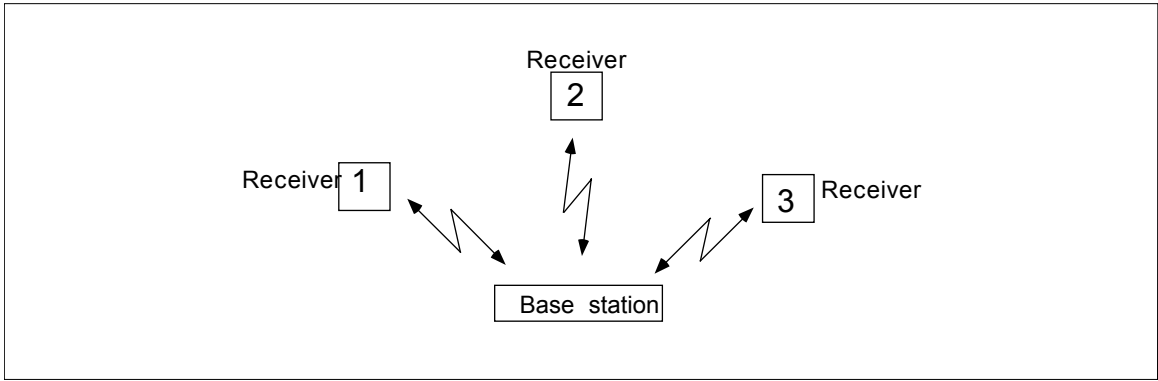


Fig39: Application overview

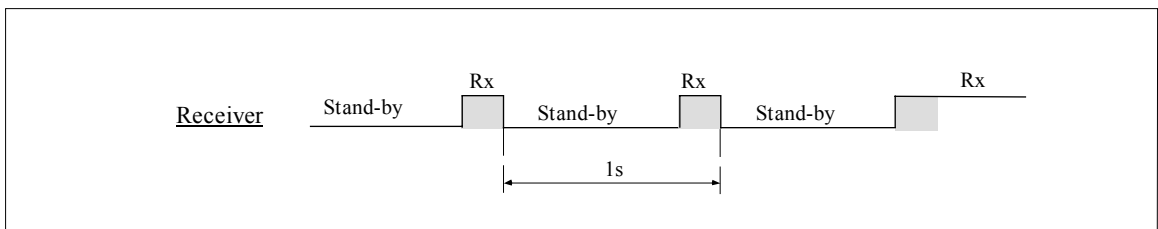


Fig40: Receiver switch

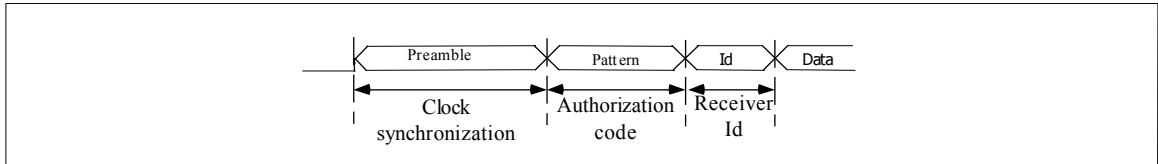


Fig41: Preamble and frame pattern

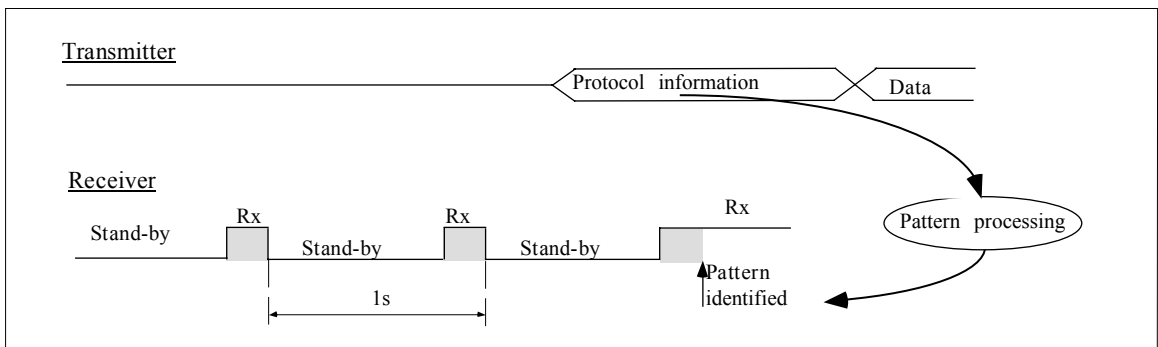


Fig42: Pattern processing

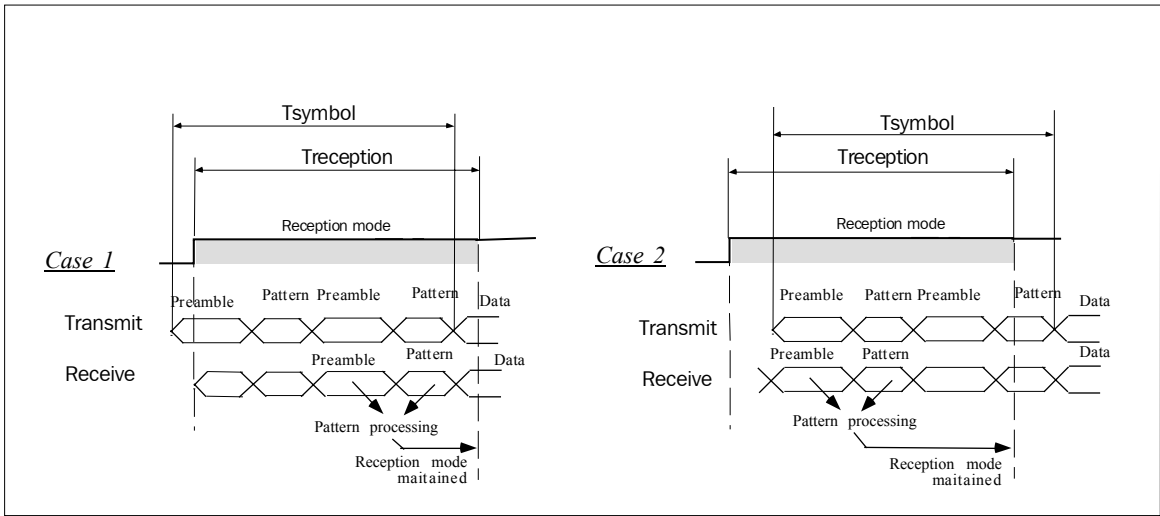


Fig45: New sequence of pattern and preamble

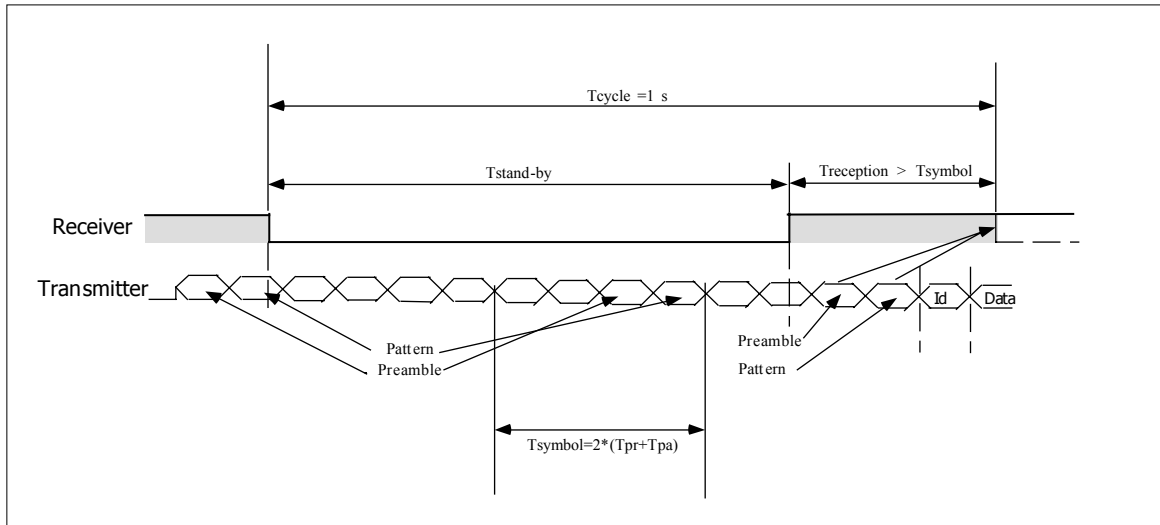


Fig 46: Timing overview

### V-3 ID processing

The transmitter sends information to a dedicated receiver. Each receiver is identified with an ID code (for example 4 bits). The ID processing is made by the micro-controller.

If the ID is correct, the receiver mode is maintained via the micro-controller, if the ID is wrong, the receiver switch to stand-by mode.

### V-4 Receiver configuration

The XE1201A is controlled via the 3-wire serial bus by a micro-controller. The Chip Enable and RxTx mode are set by hardware via the micro-controller (fig47).

3-Wire serial bus

- DE : Bus Data Enable
- SC : Serial Clock
- SD : Serial Data

Input/Output pins

- RXD : Receive data output
- CLKD: Receive data clock
- EN : Chip Enable
- RXTX : Receiver/transmitter enable

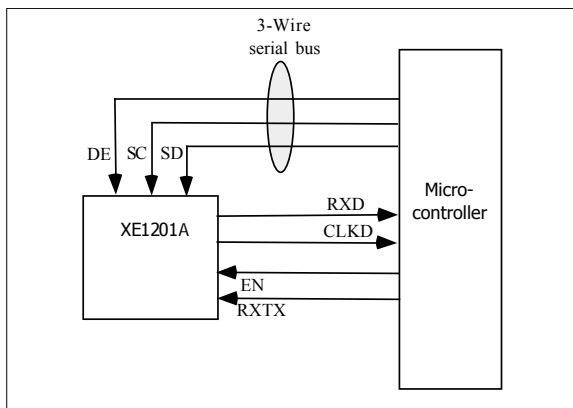


Fig47: Receiver interfaces

#### Communication diagram (fig48):

Stand-by to receiver mode:

The receiver is set in stand-by mode with clock off, the 3-wire bus set the clock on, and the micro-controller enables the chip via pin 1. The receiver is active.

Receiver to stand-by:

The receiver is in active mode, the micro-controller disables the receiver via pin 1 and the 3-wire bus switch the clock off. The chip is disable before the clock for a better power management (Receiver mode =6mA and clock running only 55uA).

#### Internal Registers configuration (fig49)

According to the receiver diagram, the 3-wire bus is used to switch on or off the internal clock of the transceiver. So only the register A (clock control bit A12) will change. The registers B and C need to be set just after the power up.

### V-5 Transmitter configuration

The XE1201A is set with clock always running, so no change is required during the transmission. This implies just one configuration via the 3-wire bus. The chip enable (PIN1) is activated by hardware via the micro-controller (fig50).

3-Wire serial bus

- DE : Bus Data Enable
- SC : Serial Clock
- SD : Serial Data

Input/Output pins:

- TXD: Data input stream
- EN: Chip Enable
- RXTX: Receiver/transmitter enable

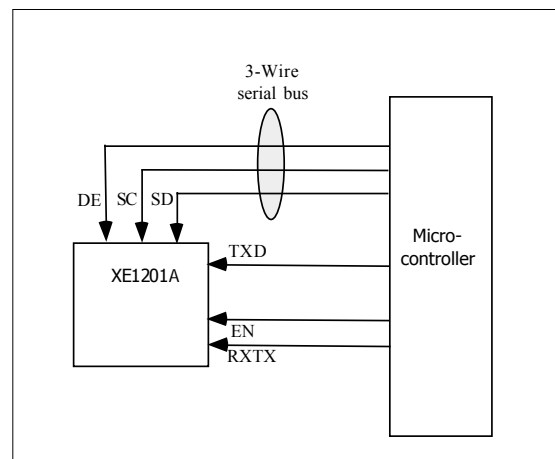


Fig50: Transmitter interface

#### Internal Registers configuration (Fig51)

The XE1201A is configured in transmitter mode with external control via pin 1 (EN) and pin 15 (RXTX). This implies A13=0. Moreover, the clock always running (A12=1), the output power is adjusted to -5dBm (C13=1, C12=1). This configuration is set just one time after the power up.

### V-6 Timing configuration

The internal demodulator of the XE1201A needs a frame of 14 synchronization bits to ensure proper clock synchronization

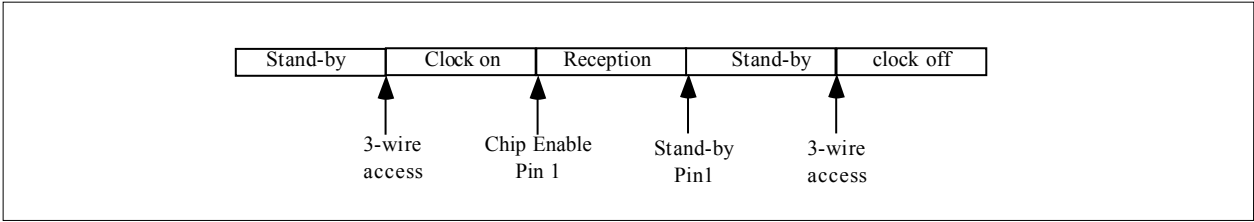


Fig48: Receiver accesses

Initialization:

Reg	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C	X	X	0	1	0	X	X	X	X	X	X	X	X	X

From stand-by to receiver mode

Reg	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	0	1	X	X	0	0	0	0	0		1	0	0	0

From receiver mode to stand-by

Reg	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	0	0	X	X	0	0	0	0	0	0	1	0	0	0

Fig 49: Receiver: Internal Register configuration

Internal Registers configuration

reg	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	0	1	X	X	X	X	X	X	X	X	X	X	X	X
B	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C	1	1	0	1	0	1	0	0	1	0	0	0	0	0

Fig51: Transmitter : Internal registers configuration

The preamble frame must be a sequence of 0 and 1 sent alternatively. The pattern frame can be a sequence of 6 bits.

$$T_{preamble} = 14 * 1/ \text{Data rate}[\text{Hz}]$$

$$T_{pattern} = 6 * 1/ \text{Data rate}[\text{Hz}]$$

With a data rate of 64kbit/s (32KHz)  
 $T_{preamble} = 437.5\mu\text{s}$   
 $T_{pattern} = 187.5\mu\text{s}$

According to the formulas below, When no data are received, the minimum time in receiver mode ( $T_{rm}$ ) is define as:

$$T_{rm} \geq 2 * (T_{preamble} + T_{pattern})$$

$$T_{rm} = 1250\mu\text{s}$$

### V-7 Current consumption and battery life

According to the data sheet and the formulas, the current evolution from stand by to receiver mode is drawing below (fig52).

In stand-by mode:

- $I_{sb} = 0.2\mu\text{A}$

Clock Wake-up:

- $I_{clk} = 55\mu\text{A}$
- $T_{clk} = 2\text{ms}$

Receiver Wake up:

- $I_{wu} = 6\text{mA}$
  - $R_{wu} = 60\mu\text{s}$
- Receiver enables:
- $I_r = 6\text{mA}$
- Where  $I_r$  is the reception current.

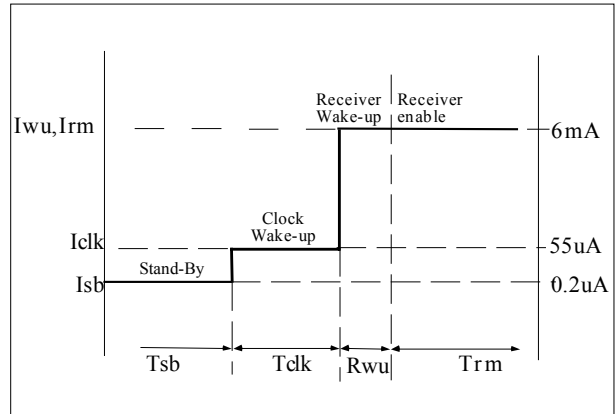


Fig52: current evolution from Stand-by mode to receiver enables

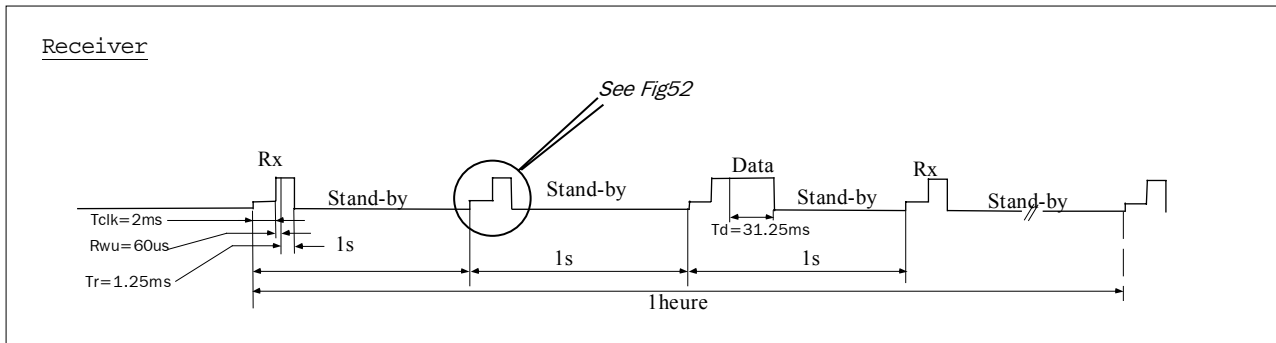


Fig53: Timing diagram of the receiver during cycle

Average current consumption per cycle when no data are received:

$$I_{av} = \left( (I_{clk} \times T_{clk}) + (I_{wu} \times R_{wu}) + (I_r \times T_{rm}) + (I_{sb} \times (1 - T_{clk} - R_{wu} - T_r)) \right)$$

$$I_{av} = 8.17\mu\text{A}$$

$$BL = \frac{300 \cdot 10^{-3}}{8.1 \cdot 10^{-6}}$$

$$BL = 4.1 \text{ years}$$

Current consumption with data received

For example the number of data to transmit is 1kbit per hour.

$T_{dr} = 31.25\text{ms}$

Where  $T_{dr}$  is the data received time

$$I_{av} = \left( \frac{(I_{clk} \times T_{clk}) + (I_{wu} \times R_{wu}) + (I_r \times T_{rm}) + (I_r \times T_{dr})}{(I_{sb} \times (1 - T_{clk} - R_{wu} - T_{rm} - T_{dr}))} \right)$$

$$I_{av} = 188\mu\text{A}$$

Battery life (BL) calculation for the XE1201A

With a battery which can deliver 300mAh

The average current with data received can be neglected So, the average current during 1 hour is around 8.1uA.

### V-8 Conclusion

This application realizes a transmission of 1kbit from a XE1201A configured in transmitter mode (fig54) to a XE1201A configured in receiver mode (fig 55) with a response time less than 1s.

As the protocol for this transmission is light and all the receivers use the bit synchronizer functionality, a low cost / low complexity micro-controller can be used. This implies for receiver functionality a current average of 8.1uA.

Note: This example shows an application with one way transmission. The half duplex transmission will be realized in the same way (fig56).



## VI - PCB guideline

A proper layout is required to obtain the optimal circuit performances. All components for tank circuits, matching network and decoupling are RF components and should be compact and placed as close as possible to the XE1201A.

The general approach to use the XE1201A and a micro-controller on the same board is to place RF on one side of the PCB (printed circuit board) and base band signal and logic circuits on the other side, with RF and logic ground planes separated

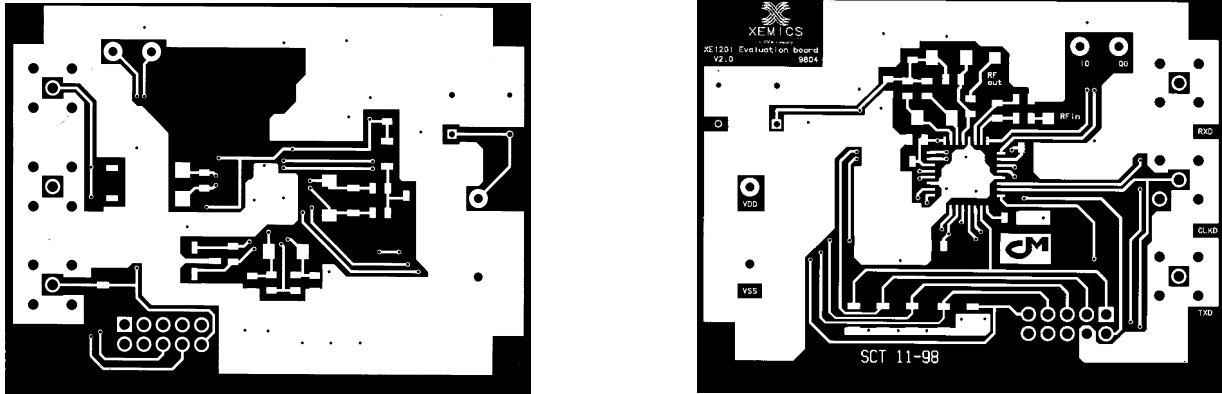


Fig53:Reference board layout

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