
AN1201A.04

Application Note

The XE1201A for Channelized applications bases on an external PLL

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INTRODUCTION

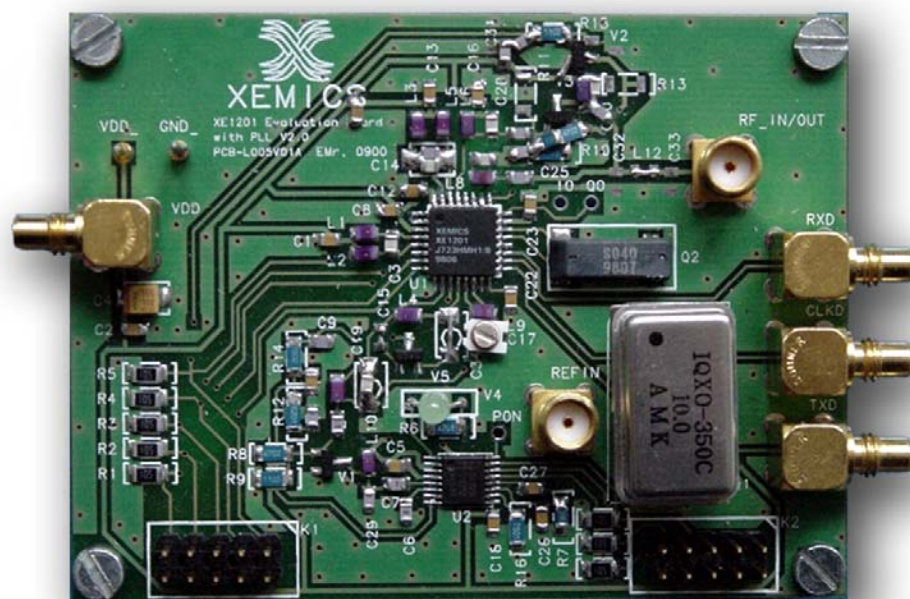
This application note describes the operations of the XE1201A for the channelized application.

The XE1201A is a half-duplex FSK single chip transceiver for operation in the 433MHz ISM band and in the 300-500MHz band. The modulation used is the Continuous Phase 2 level Frequency Shift Keying (CPFSK).

Normally built to operate with a SAW resonator that generates the Local Oscillator frequency, the XE1201A is connected to an external frequency synthesizer for channelized application.

To access the [XE1201A Datasheet](http://www.xemics.com/downloaddata.html), simply download it from XEMICS' web site:

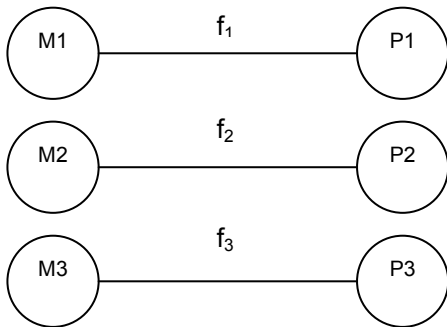
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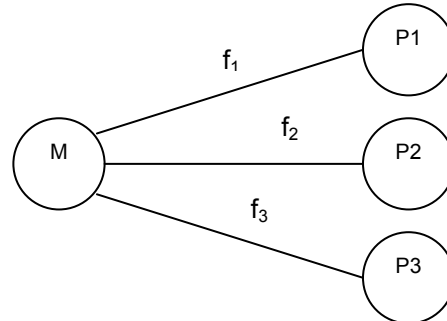
I. Typical Applications

Typical application configurations have been illustrated below:

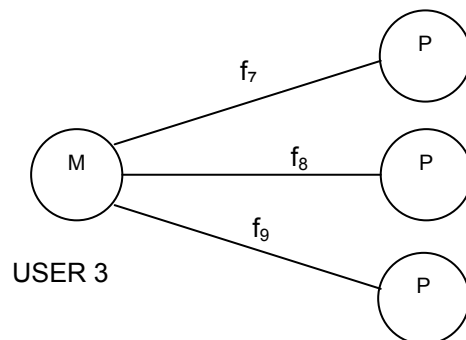
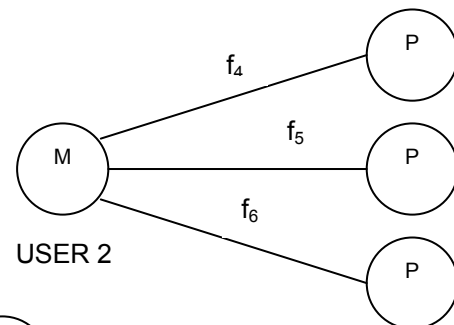
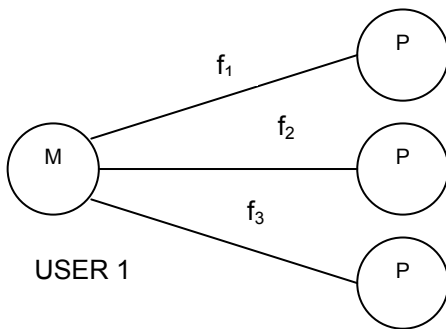
I – 1. Multi point to point communication.



I – 2. Star Network



I – 3. Multi Users concept



II. General Description of the PLL

XEMICS has developed an application board in order to give better support with perfect evaluation.

This application board is based on the transceiver XE1201A and frequency synthesizer from Philips, the SA7016. The internal VCO of the XE1201A (Voltage Control Oscillator) is used for the PLL (Phase Lock Loop).

II - 1. Functional Overview

The Figure below (Fig1) shows the typical structure of a Phase Lock Loop (PLL), which constitutes of 6 main blocks.

VCO:

This block generates the Local Oscillator inside the XE1201A. The frequency depends on the input voltage. Two varicaps plus the XE1201A constitute this block. The signal V_Tune, controls the output frequency and comes from the Charge Pump (block of the synthesizer).

Main Divider:

This block achieves a frequency division by M of VCO output (Flo). This frequency (Flo) corresponds of the Local Oscillator value. The Main Divider output is connected to the Phase

Frequency Divider block (PFD) to compare its phase between with a reference signal.

Reference Divider

As the Main Divider function, this block divides frequency of the reference signal (Fref). The output is connected to the Phase Frequency Divider block (Finter1).

Phase Frequency Divider (PFD)

The Phase Frequency Divider achieves a comparison between the two frequencies, the Main divider output (Fmain) and the Reference Divider. The result of this operation is a signal proportional to the phase error between the two inputs. This signal is used to indicate which compensation needs to be applied to the VCO via the Charge Pump and the loop Filter.

Charge Pump and Loop Filter:

This block achieves the VCO control via the output signal V_Tune. The output depends of the result of the Phase Frequency Divider. The components of the loop filter are calculated to define the current signal from the Charge Pump, the filter bandwidth and the frequency step.

A simple RC filter is added for removing harmonics.

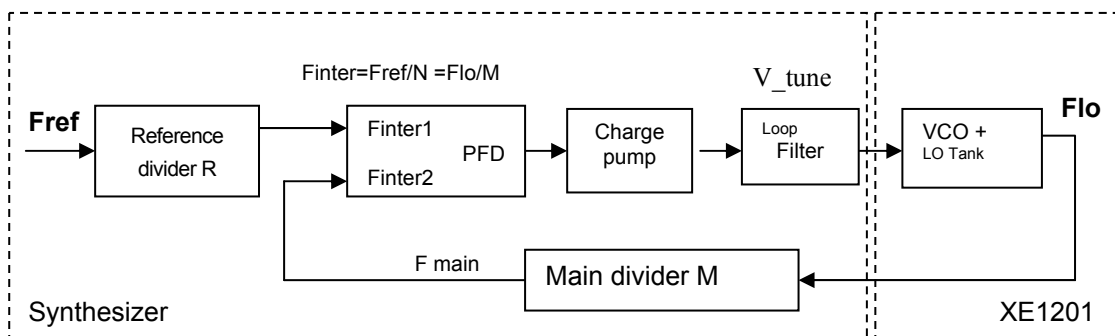


Figure 1: Schematic block of a PLL

II - 2. Charge Pump Principle

The Charge pump can be represented by the following schematic (Fig 2). Two current sources, a RC filter and a capacitor constitute the functional block of the Charge Pump.

Two different cases can be described.

- $F_{inter1} > F_{inter2}$
 - S1 is opened and S2 is closed \Rightarrow the capacitor C2 is charged by the current Ip1 and making the voltage V_Tune increase. \Rightarrow The Flo frequency from the VCO increases.
- $F_{inter1} < F_{inter2}$
 - S1 is closed and S2 is opened \Rightarrow the capacitor C2 is discharged via the current Ip2 and making the voltage V_Tune decrease. \Rightarrow The Flo frequency from the VCO decreases.

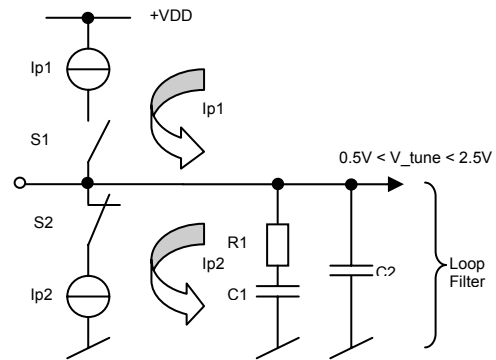


Figure 2: Functional block of the Charge Pump

III. External Components

III - 1. Tank VCO

A resonant circuit LC (Figure 3) is connected between TKA and TKC (pins 10 and 12 of the XE1201A) in order to control the VCO. This resonant circuit is calculated to obtain the Local Oscillator value required.

The signal coming from the synthesiser (V_Tune) controls the frequency oscillation via two varicaps and a parallel inductor. Because the signal V_Tune modifies the capacitor value of the varicap it also modifies the frequency of the resonant circuit

The resonant circuit, constitute L2 and C2, allows a biasing of the TKB pin to be achieved. This circuit also influences the output frequency.

On the pins SWA and SWB, a resonant circuit is also connected (L3 C3). This circuit replaces the 433MHz SAW resonator.

External components values for TKB biasing:

With Flo = 433.92MHz
 And C2 = 2-6pF ⇒ 4pF

By using the following formula, L2 can be defined as:

$$L_2 = \frac{1}{\omega^2 C_2} = 33.6nH$$

L2 = 33nH
 C2 = 2-6pF

External components values L1 and Cv

With Flo = 433.92MHz
 And C = 3 – 6pF ⇒ 4pF

By using the following formula, L1 can be defined as:

$$L_1 = \frac{1}{\omega^2 C_v} = 44.8nH$$

L3 = 39nH
 C3 = 2-6pF

External components values L3 and C3

With Flo = 433.92MHz
 And C2 = 2-6pF ⇒ 4pF

By using the following formula, L2 can be defined as:

$$L_3 = \frac{1}{\omega^2 C_3} = 33.6nH$$

L3 = 33nH
 C3 = 2-6pF

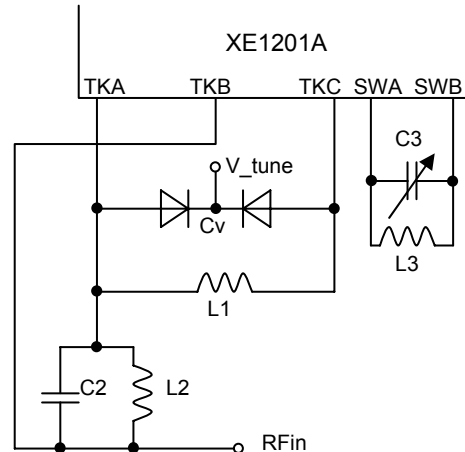


Figure 3: VCO tank circuit

III - 2. Synthesizer

VCO Gain: K_{VCO}

The external components for the VCO tank have been defined. In this case, the VCO gain can be calculated by applying a signal V_Tune and measuring the Local Oscillator value.

The objective is to obtain $f_{lo}=433.92MHz$ for $V_Tune = V_{dd}/2$

The Figure 4 below shows how to determine the K_{VCO} .

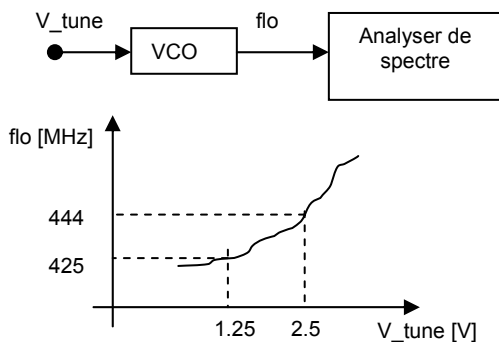


Figure 4: K_{VCO} measurement

$$K_{VCO} = \frac{f_2 - f_1}{V_2 - V_1} = 14.5MHz/V$$

Phase Detector Gain: $K\Phi$

The charge pump current values (I_{cp}) are determined by the current at pin Rset (pin10) in conjunction with internal bits of the SA7016.

From the datasheet of the SA7016, Rset is fixed to 7.5K Ohm for a voltage of 1.25V.

And with $C_p=0$, the charge pump current is determined as following:

$$I_{cp} = 3.I_{set} = \frac{3.V_{set}}{R_{set}} = \frac{3 \times 1.25}{7.5 \cdot 10^3} = 500\mu A$$

The charge pump current can be modified via the Philips control program for the frequency synthesiser SA7016.

And So:

$$K\Phi = \frac{I_{cp}}{2\pi} = 500\mu A / rad$$

Damping Factor: ξ

$$\xi = 0.707$$

Main Divider: M

With:

$$F_{inter} = 500kHz$$

$$f_{lo} = 433.92MHz$$

The main divider is defined as following:

$$M = \frac{f_{lo}}{F_{inter}} = 868 = 1101100100b$$

Reference divider: R

The PFD inputs need to respect the following equations:

$$F_{inter1} = F_{inter2} = 500kHz$$

and

$$F_{inter1} = \frac{F_{ref}}{R}$$

The reference divider consists of a divider with programmable values between 4 and 1023 followed a three bit binary counter. The 3 bits register determines which of the 5 output pulses are selected as the main/auxiliary detector input. For more information refer to the SA7016 Datasheet.

The reference-input signal has been fixed at 10MHz.

So with: $R[4...1023]$

The reference divider is defined as following:

$$R = \frac{F_{ref}}{F_{inter}} = \frac{10 \cdot 10^6}{500 \cdot 10^3} = 20 = 10100b$$

Loop Filter

The structure of this filter is shown in the figure below:

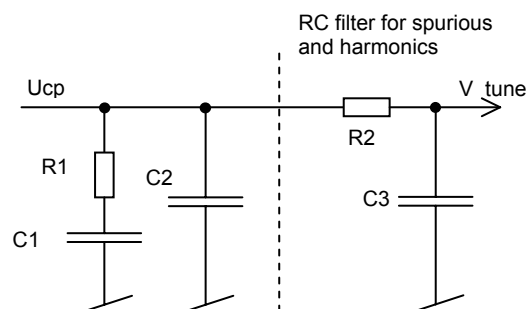


Figure 5: Loop filter structure

Loop filter Design Equations:

δ : Final frequency resolution after settling

$$\delta = \frac{\text{frequency error after settling}}{\text{switching time}} \quad (1)$$

t_{sw} : Switching time ($t_{sw}=400\mu s$)

f_n : Natural frequency

$\omega_n = 2\pi f_n$ (rad/sec)

ζ : Damping Factor

$$\omega_n = \frac{-\ln(\delta \cdot \sqrt{1-\zeta^2})}{\zeta \cdot t_{sw}} \quad (2)$$

$$C_1 = \frac{K\phi \cdot K_{VCO}}{N \cdot \omega_n^2} \quad (3)$$

$$R_1 = 2 \cdot \zeta \left(\frac{N}{K\phi \cdot K_{VCO} \cdot C_1} \right)^{0.5} \quad (4)$$

$$C_2 \leq \frac{C_1}{10} \quad (5)$$

$$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_n \quad (6)$$

Design example:

Frequency error = within 1kHz

Switching time = 400 μ s

K_{VCO} = VCO gain

$K\phi$ = Phase detector gain

From the equation (1) and with the condition above:

$$\zeta = \frac{1000}{400 \cdot 10^{-6}} = 0.04 \cdot 10^{-3}$$

From the result of the equation (1) and with the equation (2), the natural pulsation can be defined as following:

$$\omega_n = \frac{-\ln(0.04 \cdot 10^{-3} \times \sqrt{1-0.707^2})}{0.707 \times 400 \cdot 10^{-6}}$$

$$\omega_n = 37.10^3 \text{ rad / s}$$

With the natural pulsation and with the phase detector gain and the VCO gain, the equation (3) defines the capacitor C_1 :

$$C_1 = \frac{500 \cdot 10^{-6} \times 14.5 \cdot 10^6}{868 \times (37.10^3)^2}$$

$$C_1 = 6.10 \text{ nF}$$

So the choice of C_1 is:

$$C_1 = 6.8 \text{ nF}$$

From the value of the capacitor C_1 , the resistor R_1 can be defined by using the equation (4):

$$R_1 = 2 \times 0.707 \cdot \sqrt{\frac{868}{500 \cdot 10^{-6} \times 14.5 \cdot 10^6 \times 6.1 \cdot 10^{-9}}}$$

$$R_1 = 6.25 \text{ k}\Omega$$

So the value of R_1 is

$$R_1 = 6.20 \text{ k}\Omega$$

The equation (5) defines the capacitor C_2 from the value of C_1 .

$$C_2 \leq \frac{6.80 \cdot 10^{-9}}{10} = 680 \text{ pF}$$

The software Winsynth from Philips (Figure 6) allows defining the values of R_2 and C_3 .

$$R_2 = 18 \text{ k}\Omega$$

$$C_3 = 150 \text{ pF}$$

Summary:

$$R_1 = 6.20 \text{ k}\Omega$$

$$C_1 = 6.8 \text{ nF}$$

$$C_2 = 680 \text{ pF}$$

$$R_2 = 18 \text{ k}\Omega$$

$$C_3 = 150 \text{ pF}$$

Winsynth: Filter Calculator

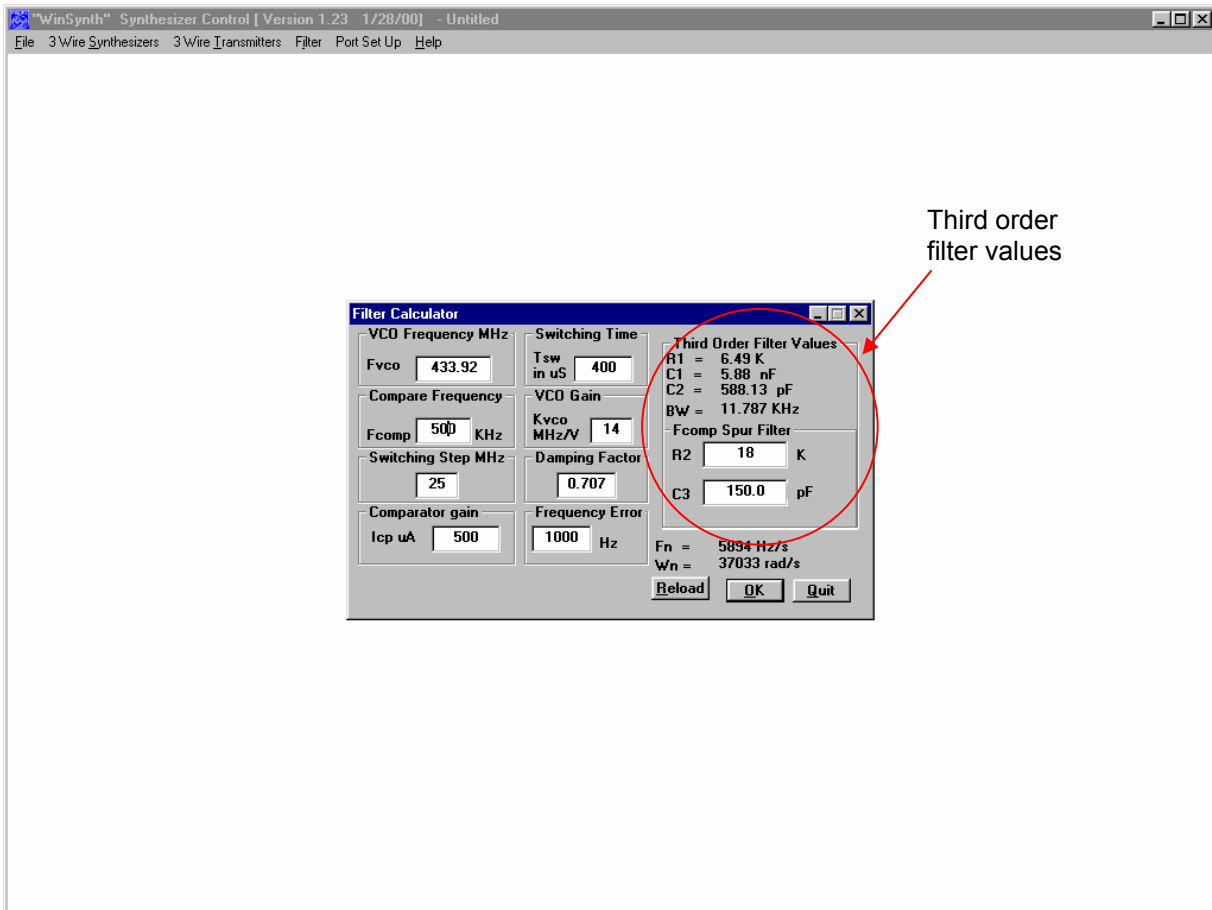


Figure 6: Filter Calculator

Decoupling Capacitors

At the Fref input:

The figure 7 below shows the decoupling capacitors for the Fref input.

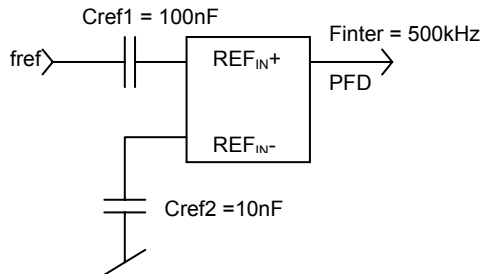


Figure 7: Fref input

At the RFIN input

The decoupling capacitor for the Rfin input is shown in the figure 8 and with its equivalent schematic.

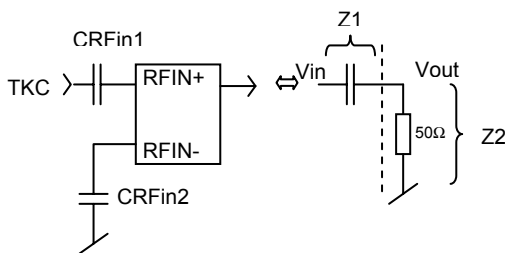


Figure 8: RFin input

The schematic is equivalent to a high pass filter for the input TKC. The choice is to have the cut-off frequency equal to the central frequency divided by 10.

So:

$$V_{out} = \frac{Z_2}{Z_1 + Z_2} V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{jRC_{RFIN1}\omega}{1 + jRC_{RFIN1}\omega}$$

$$\omega_{cut_off} = \frac{1}{RC_{RFIN1}}$$

$$C_{RF\,int1} = \frac{1}{2\pi \cdot f_{cut_off} R} = 74\,pF$$

with

$$\omega_0 = 2\pi f_0$$

$$f_0 = 433.92\,MHz$$

$$f_{cut_off} = 43.92\,MHz$$

III - 3. External Power amplifiers

The RF_{in+} input of the Philips synthesiser, the SA7016, accepts a signal level of -18dBm min. The signal, coming from TKB of the XE1201A, has a maximum level of -29dBm. A power amplifier was designed to increase the RF signal level at the SA7016 input, up to -18dBm. This external power amplifier (Figure 9) needs to have a gain higher than 12dB.

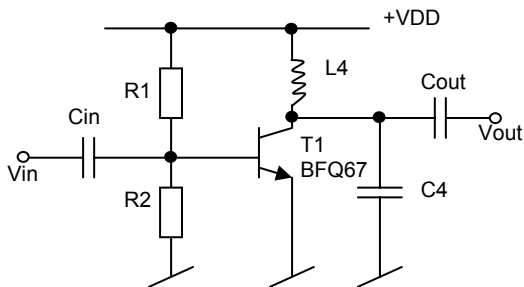


Figure 9: Power Amplifier for the synthesiser

The two components L4 and C4 are equivalent to a resonant circuit at the F_{lo} frequency.

The capacitor C4 is defined as follows:

$$L_4 \cdot C_4 \cdot \omega_0^2 = 1$$

With :

$$L_4 = 18nH \quad \text{and} \quad F_{lo} = 433.92MHz$$

$$C_4 = \frac{1}{(2\pi \cdot 433.92 \cdot 10^6)^2 \cdot 18 \cdot 10^{-9}} = 7.47pF$$

The two resistors R1 and R2 were chosen in order to create a gain between Vin and Vout higher than 12dB and using a low current consumption. The result is:

$$R1=47k\Omega$$

$$R2=110k\Omega$$

For a current consumption of: 5mA and a Gain of 12.5dB.

Capacitors Cin and Cout

The two-capacitor values need to be defined by using high pass filter equivalent schematics with R1 and R2. The added noise due to the Power amplifier needs to be minimised.

In this case:

$$Cin=1pF$$

$$Cout=100pF$$

A second power amplifier (Figure 10) has been added in order to obtain +7.5dBm output power instead of 5dBm (typical output power value of the XE1201A).

So this power amplifier needs to have a gain of 10dB and to resonate at 433.92MHz. In order to optimise the power consumption the amplifier needs to be switched off when the XE1201A is configured in receiver mode. In this case this structure can also be used as an external switch between Transmit and Receive. The RxTx signal comes from the microcontroller and is used to program the transceiver XE1201A. It also used to manage the external switch. This reduces the number of external components and uses only one antenna.

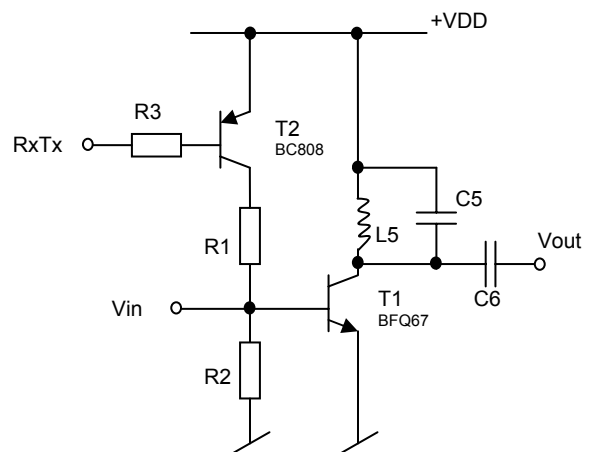


Figure 10: Power Amplifier for the XE1201A

How it works:

If the signal RxTx is equal to zero, the transistor T2 is saturated. In this case the V_{R1} equal V_{dd}-V_{CE2}, and the transistor T1 with L5, C5 will amplify the signal Vin.

If RxTx is equal to V_{dd} (High logic level), the transistor T2 is blocked and V_{be} of T1 is equal to 0V. T1 is also blocked.

External component values:

$$R1=47k\Omega$$

$$R2=100k\Omega$$

$$R3=47k\Omega$$

$$L5=18nH \text{ (choice)}$$

For the 50Ω load

$$C5=1.5pF$$

$$C6=3.3pF$$

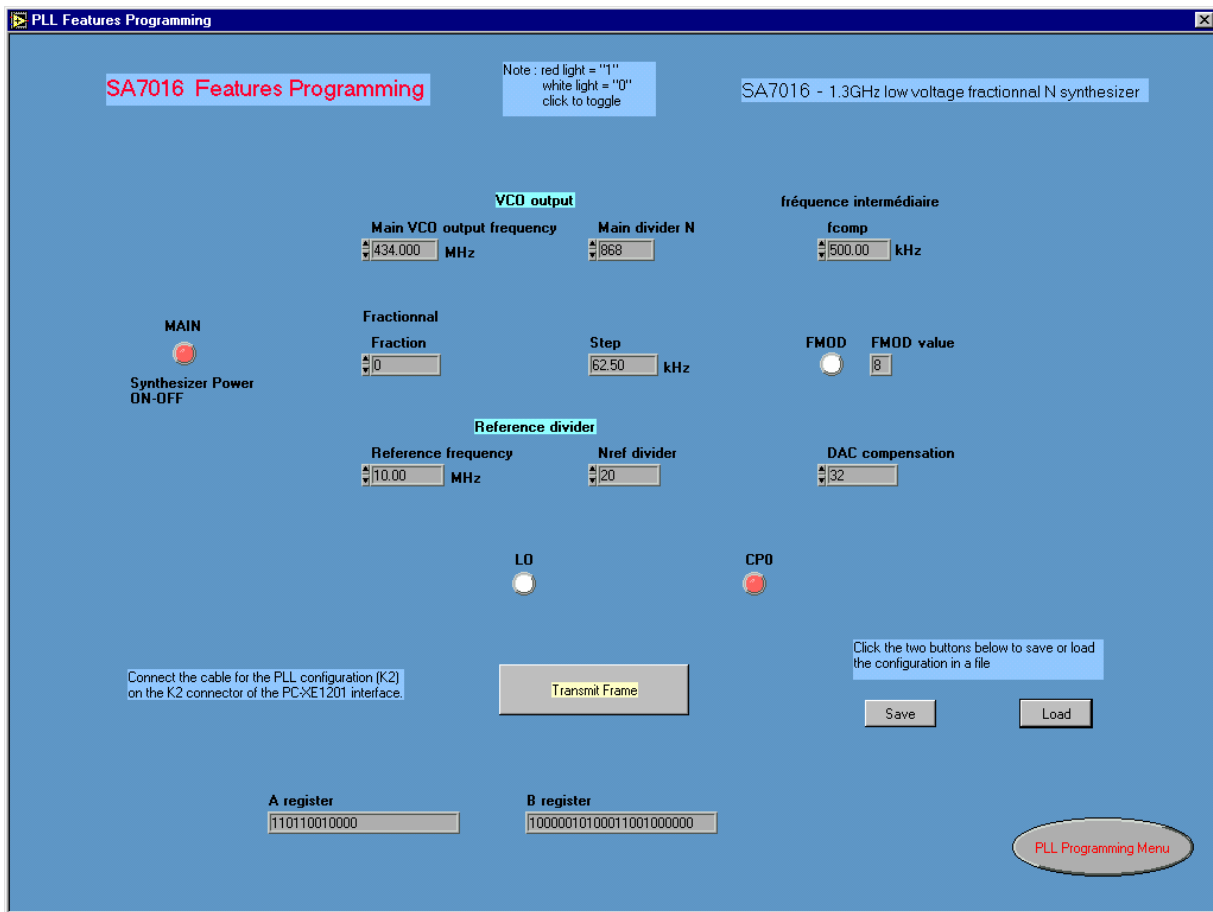
IV. Set-up

The performances of the XE1201A with an external PLL can be directly evaluated via a reference board. For better "ease of use" XEMICS has developed its own software to program the transceiver and the PHILIPS synthesiser.

For more information about the XE1201A set-up refer to the XE1201AEVK User Guide at:
<http://www.xemics.com>

The XEMICS software allows SA7016 programming. A typical configuration is shown in Figure 11. All the parameters are accessible, for example:

- VCO output (434MHz Typical value)
- Main Divider (M)
- Intermediate frequency (Fcomp)
- Step
- Reference frequency
- Ref Divider (R)



V. Measurement

V - 1. Configuration

The XE1201A with an external synthesiser is set-up with the following configuration:

Frequencies :

$$f_{LO} = 433.92MHz$$

$$f_{ref} = 10MHz$$

$$f_{inter} = 500KHz$$

Divider :

$$M = 868 = 1101100100b$$

$$R = 20 = 10100b$$

PLL

$$Step = \frac{f_{inter}}{8} = 62.5kHz \quad f_{mod} = 0$$

$$CP = 1$$

V - 2. Current consumption

To evaluate the performances of the complete systems, the current consumption is measured in the three different modes: Stand-by, receiver and transmitter mode. These measures have been made at 3V and with a temperature of 20°C.

Stand-by mode	< 100µA
Receiver mode	19.25mA
Transmitter mode:	-10dBm: 23mA
	-5dBm: 24mA
	0dBm: 25mA
	+5dBm: 26mA

V - 3. RF performances

In receiver mode

$$\text{Sensitivity} = -103dBm @ 16kbps$$

In transmitter mode

-10dBm programmed	-5dBm measured
Gain=5dB	

-5dBm programmed	-1.5dBm measured
Gain=3.5dB	

0dBm programmed	2.5dBm measured
Gain=2.5dB	

+5dBm programmed	7.5dBm measured
Gain=2.5dB	

V - 4. Phase noise of the PLL

The following formula and the Figure 12 are used to calculate the phase noise of the PLL.

$$PN = dPN @ 100kHz - 10 \log RBW$$

With

RBW : Resolution Bandwidth

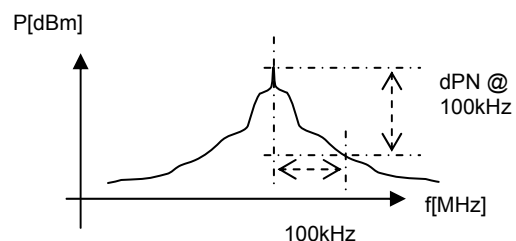


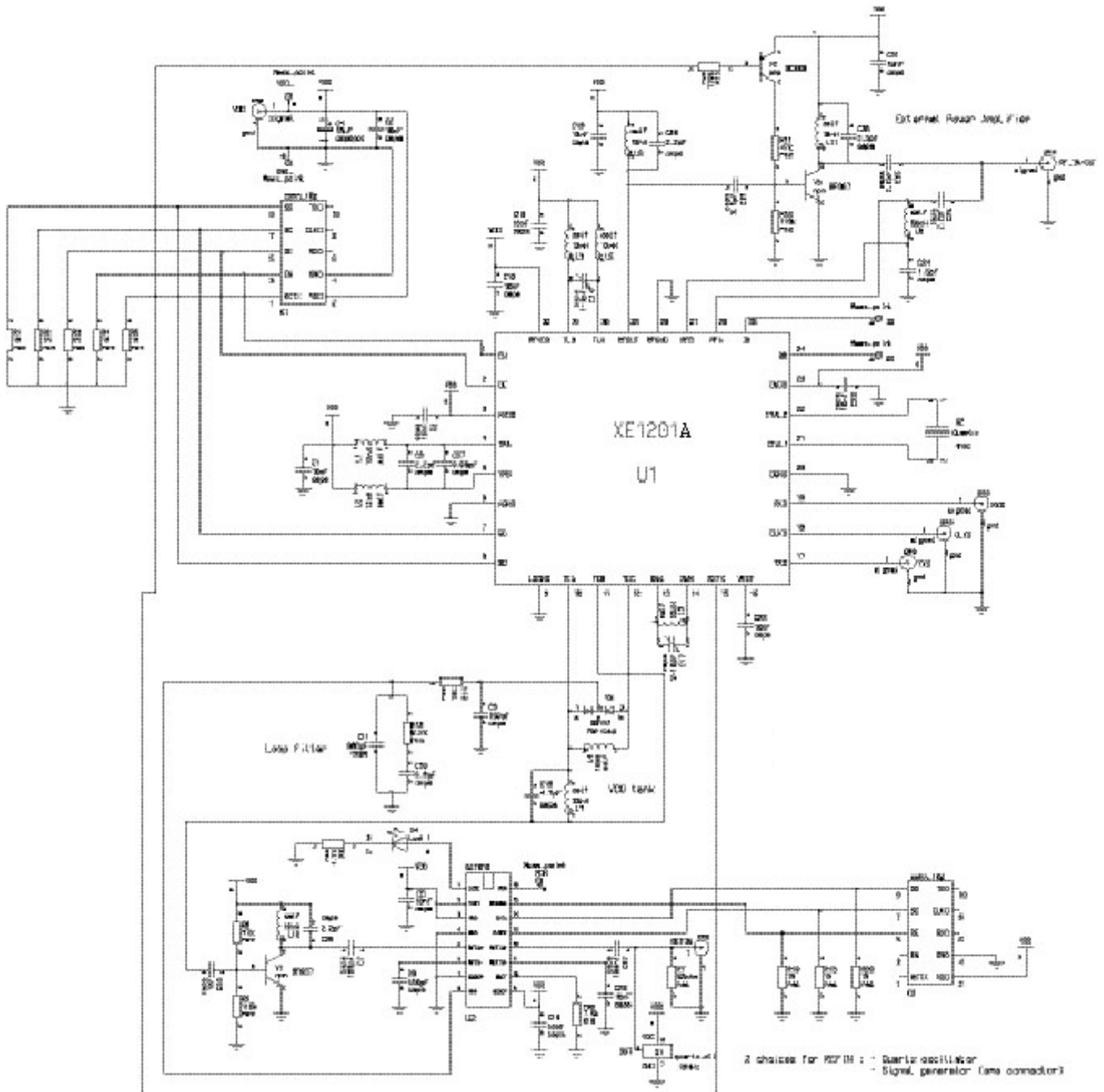
Figure 12: Phase Noise measurement

$$PN = -42.89 - 10 \log(100 \cdot 10^3) = -92.9dBm$$

Note: The Phase noise has been calculated at the Power Amplifier output. This block has also added some phase noise.

Exhibit I: Bill of material

Name	Type	Reference	Value	Form	Quantity
U1	XE1201A Transceiver IC	XE1201A-T		TQFP32	1
U2	Synthesizer	SA7076		SOT403-1	1
Q1	XTAL Quartz	AMK - IQXO-350C	10I00MHz	-	1
Q2	XTAL Quartz	S0409745	4.00MHz	-	1
V1	NPN Transistor	BFQ67		Sot23	1
V2	PNP Transistor	BC808		Sot23	1
V3	NPN Transistor	BFQ67		Sot23	1
V4	LED				1
Varicap		BBY51			1
C4	Decoupling capacitor		10uF		1
C28	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	1nF	SMD0805	1
C2	Decoupling capacitor		10nF		1
C1, C5, C8, C12, C13, C16, C18, C22, C23, C26, C31	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	10nF	SMD0805	11
C27	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	100nF	SMD0805	1
C25, C30	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	1.5pF	SMD0805	2
C3, C20, C21, C24, C35	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	2.2pF	SMD0805	5
C17	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	3.3pF	SMD0805	1
C10	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	6.8pF	SMD0805	1
C6,C7, C15	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	100pF	SMD0805	3
C9,	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	150pF	SMD0805	1
C11,	Capacitor 0805	805 NPO Ni, +/-0.25pF, 50v	680pF	SMD0805	1
C14	Trim-Capacitor	TZC03Z060A110	1 to 3pF	SMD0805	1
C19, C34	Trim-Capacitor	TZC03Z060A110	2 to 6pF	SMD0805	2
L1, L2, L3, L5	self	0805 CS-120-X JBC 5%	12nH	SMD0805	4
L6, L11	self	0805 CS-180-X JBC 5%	18nH	SMD0805	2
L10	self	0805 CS-220-X JBC 5%	22nH	SMD0805	1
L4	self	0805 CS-270-X JBC 5%	27nH	SMD0805	1
L7, L9	self	0805 CS-330-X JBC 5%	33nH	SMD0805	2
L8	self	0805 CS-560-X JBC 5%	56nH	SMD0805	1
R7	Load	any	50	SMD1206	1
R6, R16	Pola resistor	any	4.7k	SMD1206	2
R12	Loop Filter	any	6.2k	SMD1206	1
R14	Loop Filter	any	18k	SMD1206	1
R8, R11	Pola resistor	any	47k	SMD1206	2
R9, R10	Pola resistor	any	110k	SMD1206	2

Exhibit II: Electrical Schematic


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